

Intel Huron River Sandy Bridge 32nm SV PGA988B i3, i5 DC 35W/ i7 QC 45W

POWER

DGPU_PWROK 56

FAN 27
Conn
Cable

KBC
ITE8518
29

Conn	PWR Button / White LED
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White: PWR on
Link White: Standby

Project Name : H710DI1	Title : Block_I
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FLEX Computing			
Project Name : H710Dh1		Title : Block_Diagram	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : A	
Date: Monday, November 08, 2010		Sheet : 1	of 63

Layout

DMI

Differential 85ohm (single 50)
n,p mismatch <5mils
maximum mis-match between inter-pairs :
7000 mils (177.8 mm)
Max: [2000 to 8000 mils, 3vias]
436735 Huron River Design Guide 1.0

Layout

FDI

Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
3vias : 2000 to 8000 mils
4vias : 2000 to 6500 mils
436735 Huron River Design Guide 1.0

Note:

FDI (Flexible Display Interface):
Carries display traffic
from the integrated graphics controller
to the legacy display connectors in the PCH.

Layout

DP_ICOMPO :

Trace Width : 12 mils (0.305 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length : 500 mils (12.7 mm)

DP_COMPIO :

PEG_RCOMPO
Trace Width : 4 mils (0.102 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length : 500 mils (12.7 mm)

436735 Huron River Design Guide 1.0

Layout

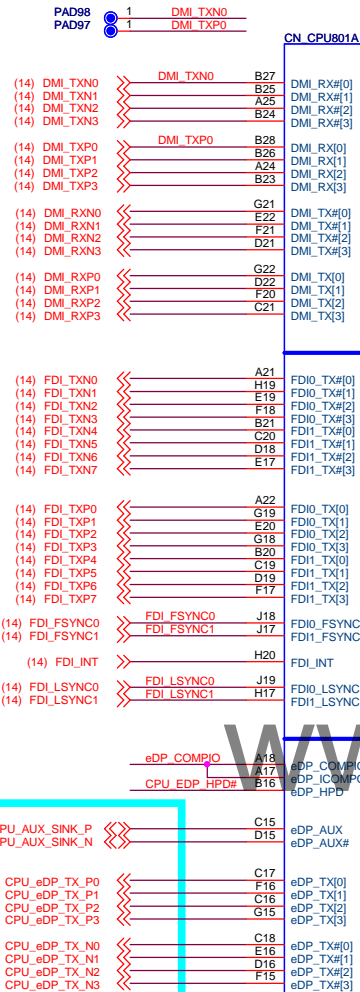
eDP

Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
2vias : 2000 - 8000 mils
4vias : 2000 - 8000 mils
436735 Huron River Design Guide 1.0

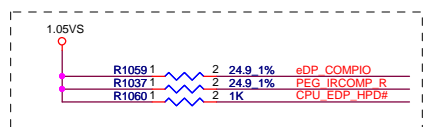
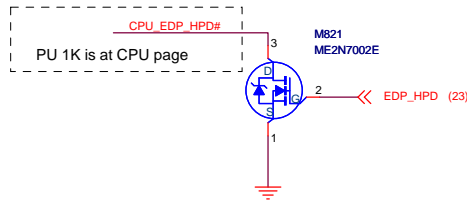
Layout(Switchable Graphics Topology)

eDP

Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
4vias : 2000 - 5000 mils
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Sandy Bridge_FOXCONN_PZ98927-3641-41F



PCI EXPRESS* - GRAPHICS

eDP

Sandy Bridge_FOXCONN_PZ98927-3641-41F

HPMH-11-0010000110G	IC CPU SNB 1G8 Q15M D0 rPGA988B
HPMH-11-0010000111G	IC CPU SNB 2G Q15C D0 rPGA988B
HPMH-11-0010000112G	IC CPU SNB 2G2 Q154 D0 rPGA988B
HPMH-11-0010000113G	IC CPU SNB 2G5 Q17N J0 rPGA988B
HPMH-11-0010000114G	IC CPU SNB 2G6 Q16P J0 rPGA988B
HPMH-11-0010000115G	IC CPU SNB 2G7 Q16M J0 rPGA988B
HPMH-11-0010000116G	IC CPU SNB 2G5 Q17N J0 rPGA988B
HPMH-11-0010000117G	IC CPU SNB 2G2 Q1CL D1 rPGA988B
HPMH-11-0010000118G	IC CPU SNB 2G3 Q1CG D1 rPGA988B
HPMH-11-0010000119G	IC CPU SNB 2G Q1CN D1 rPGA988B
HPMH-11-0010000120G	IC CPU SNB 2G Q1NS D2 rPGA988B
HPMH-11-0010000121G	IC CPU SNB 2G2 Q1NN D2 rPGA988B
HPMH-11-0010000122G	IC CPU SNB 2G3 Q1NC D2 rPGA988B
HPMH-11-0010000123G	IC CPU SNB 2G1 Q1SP J1 rPGA988B
HPMH-11-0010000124G	IC CPU SNB 2G3 Q1SD J1 rPGA988B
HPMH-11-0010000125G	IC CPU SNB 2G5 Q1RX J1 rPGA988B
HPMH-11-0010000126G	IC CPU SNB 2G6 Q186 J1 rPGA988B
HPMH-11-0010000127G	IC CPU SNB 2G7 Q1S2 J1 rPGA988B
HPMH-11-0010000128G	IC CPU SNB 2G SR02Y D2 rPGA988B
HPMH-11-0010000129G	IC CPU SNB 2G2 SR014 D2 rPGA988B
HPMH-11-0010000130G	IC CPU SNB 2G3 SR012 D2 rPGA988B

Layout

PEG_ICOMPO :

Trace Width : 12 mils (0.305 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length : 500 mils (12.7 mm)

PEG_ICOMPI :

Trace Width : 4 mils (0.102 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length : 500 mils (12.7 mm)

436735 Huron River Design Guide 1.0

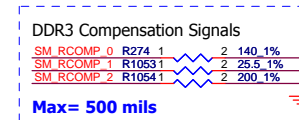
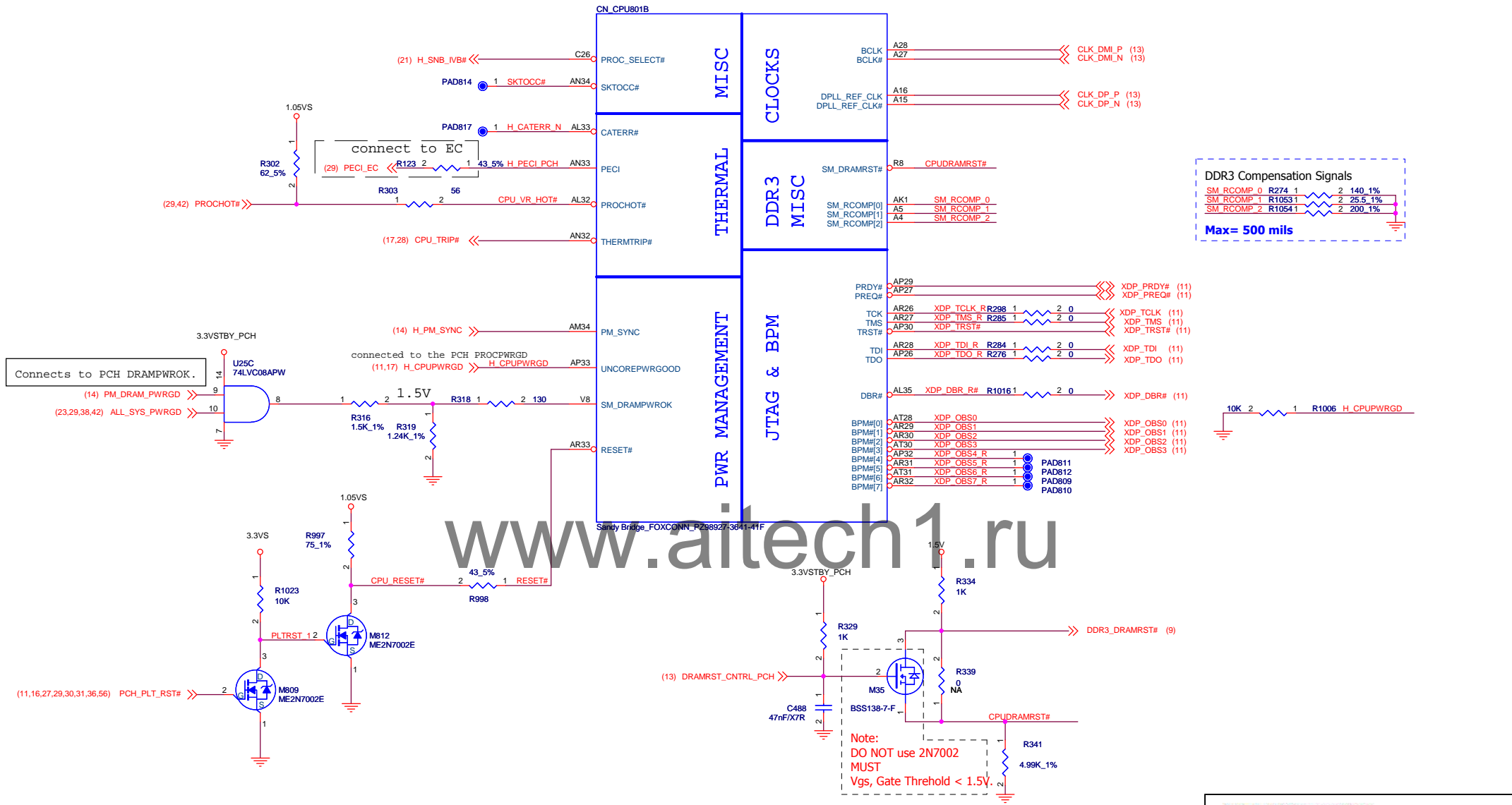
Layout

Intel PEG
Differential 80ohm(single 48ohm)

The change in AC capacitor value from 100nF to 220nF
is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

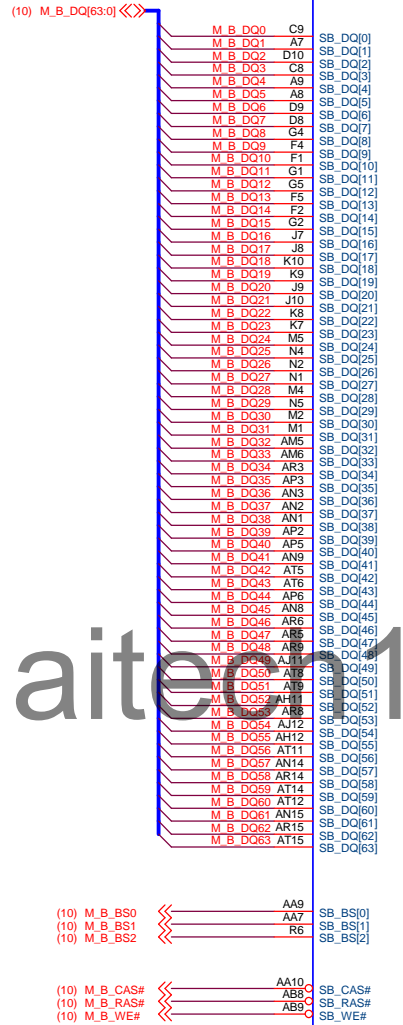
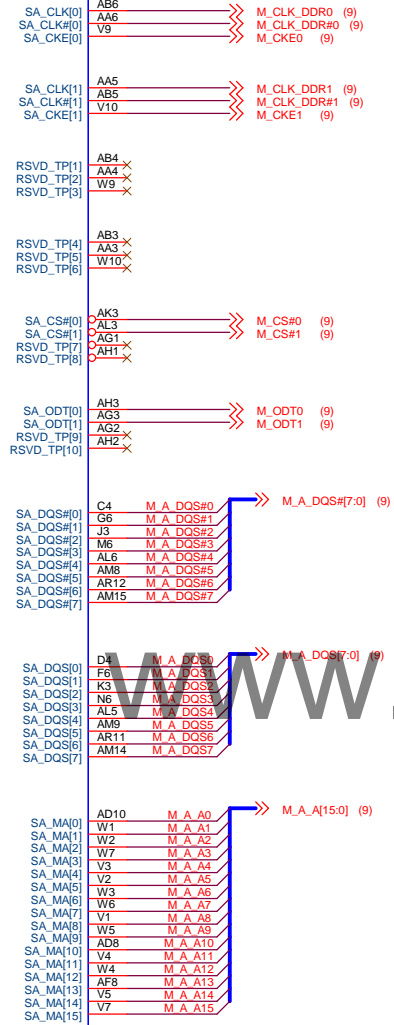
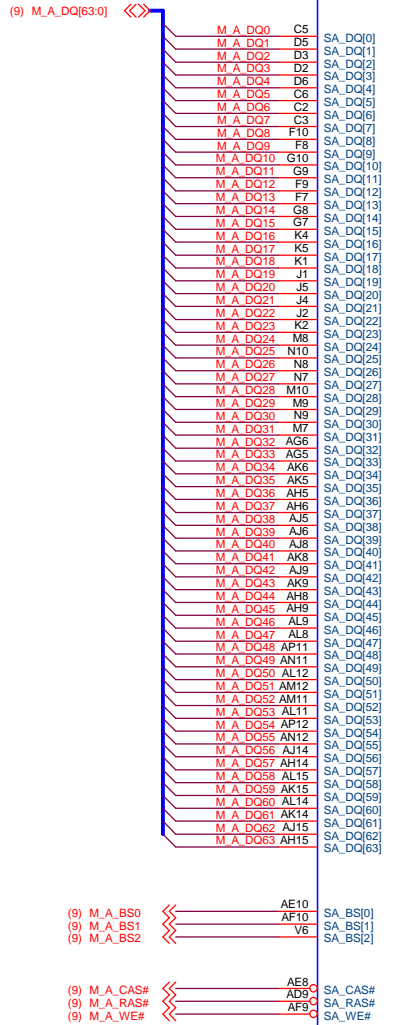
FLEX Computing

Project Name : H710DI1	Title : CPU_1/7_DMI_FDI_PCIE
Size : Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet: 2 of 63

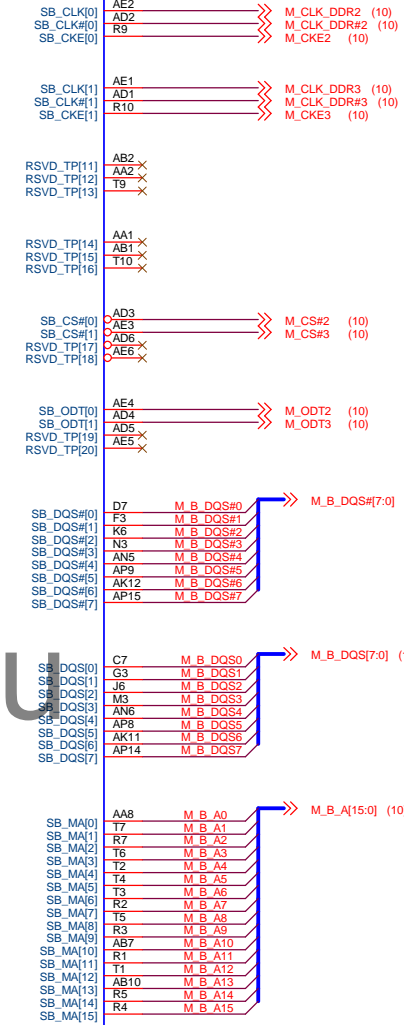


FLEX Computing			
Project Name :		Title :	
H710DI1		CPU_2/7_CLK_MISC_THERM	
Size :	Document Number :		Rev :
	HPMH-40GAB6600-B130		B
Date: Monday, November 08, 2010		Sheet :	3 of 63

DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

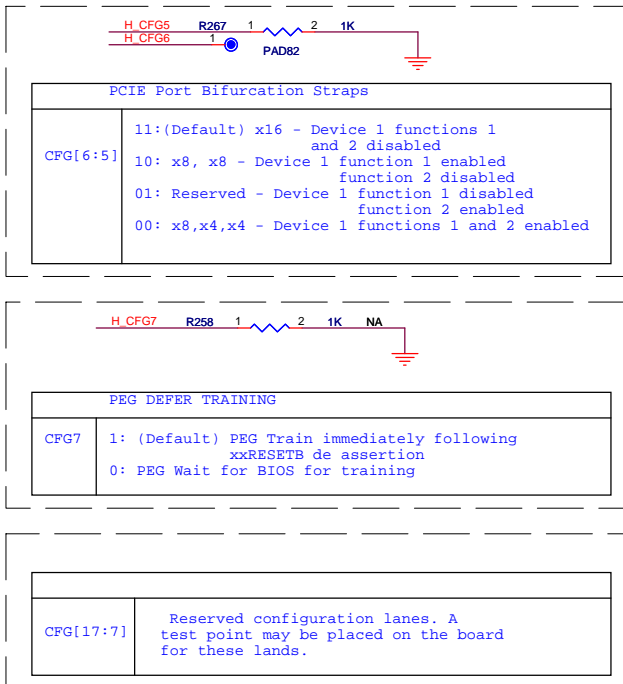
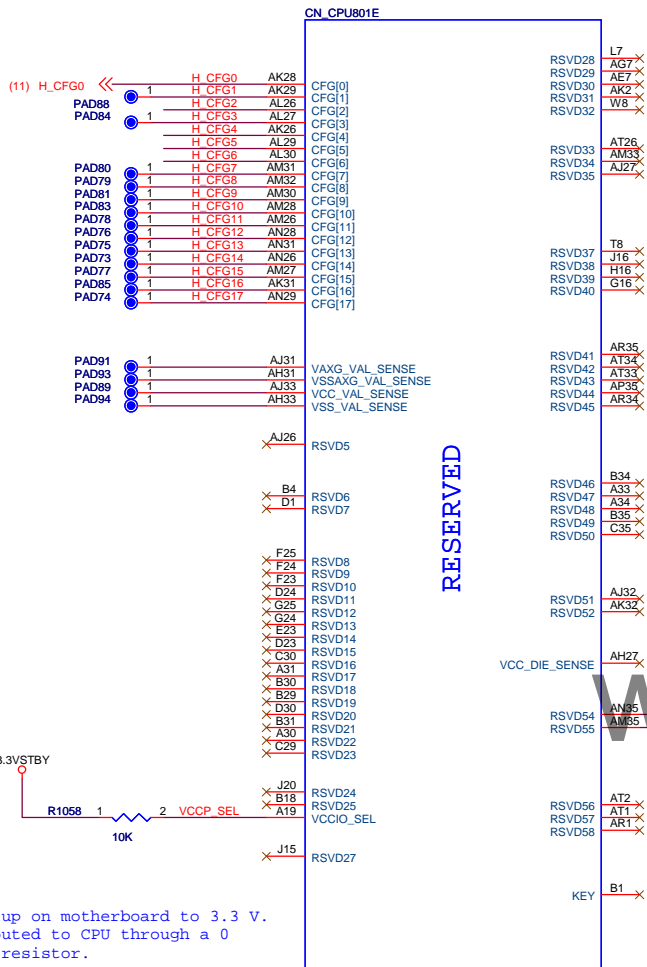


Sandy Bridge_FOXCNN_PZ98927-3641-41F

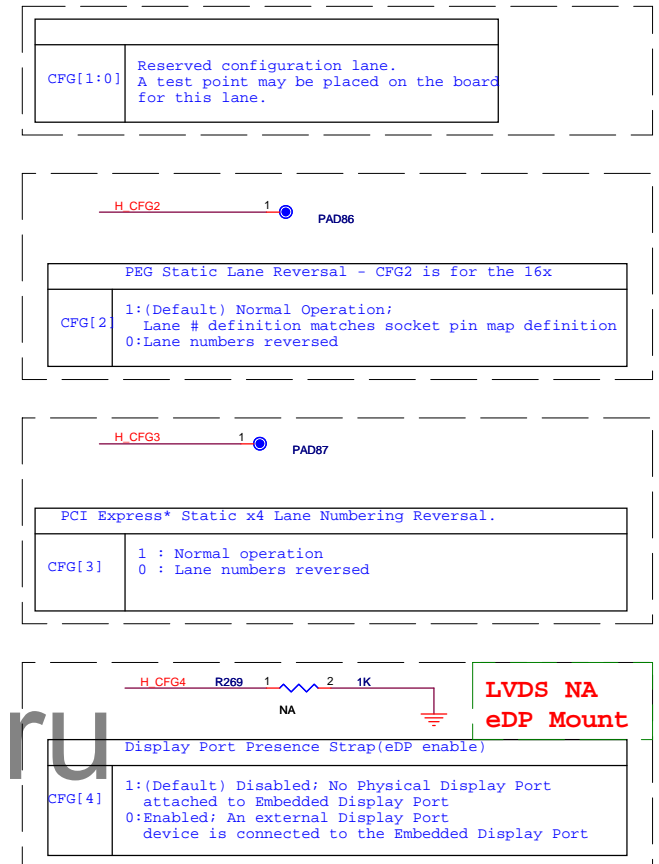
Sandy Bridge_FOXCNN_PZ98927-3641-41F

FLEX Computing

Project Name : H710D11		Title : CPU_3/7_DDR3	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 4	of 63



CFG Straps for PROCESSOR



www.aitech1.ru

Pulled up on motherboard to 3.3 V.
 Also routed to CPU through a 0 series resistor.

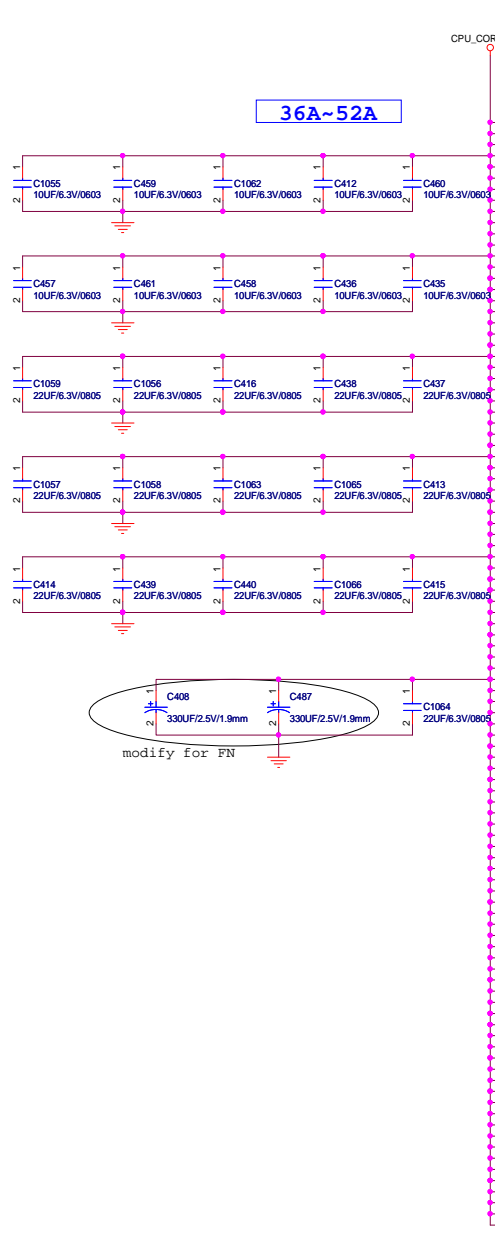
VCCIO_SEL On CRB
 H_SNB_IVB#_PWRCTRL = low, 1.0V
 H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

Voltage selection for VCCIO: For Huron
 River platforms, this pin must be pulled high
 on the motherboard

FLEX Computing

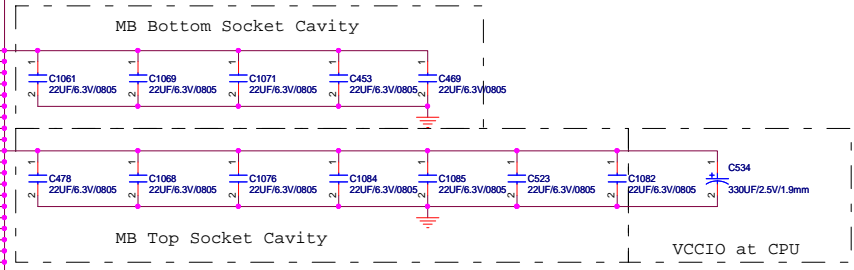
Project Name : H710DI1 Title : CPU_4/7_RSVD_CFG

Size : Document Number : HPMH-40GAB6600-B130 Rev : B
 Date: Monday, November 08, 2010 Sheet : 5 of 63



36A~52A

8.5A



7/06 delet 330uF X2
poewr side have 330uF X3
(3x 330 μ F for 2012 capable designs)
follow Huron River Platform Power Delivery (439028)

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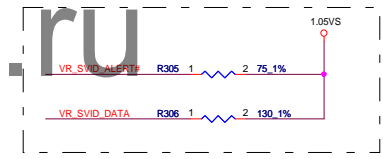
CORE SUPPLY

SVID

SENSE LINES



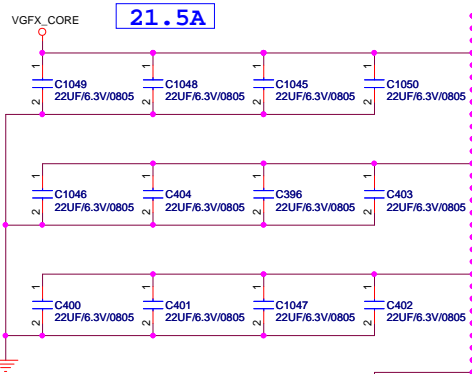
Layout Note:
Alert#(AJ29) signal must be routed between
the Clock and Data lines to reduce the cross
talk between them. Spacing recommendations
from the "Asynchronous Signal General
Routing Guideline" of the Huron River
PDG have to be met.



Sandy Bridge_FOXCONN_P298927-3641-41F

POWER

CN_CPU801G



AT24 VAXG1
AT23 VAXG2
AT21 VAXG3
AT20 VAXG4
AT18 VAXG5
AT17 VAXG6
AR24 VAXG7
AR23 VAXG8
AR21 VAXG9
AR20 VAXG10
AR18 VAXG11
AR17 VAXG12
AP24 VAXG13
AP23 VAXG14
AP21 VAXG15
AP20 VAXG16
AP18 VAXG17
AP17 VAXG18
AN24 VAXG19
AN23 VAXG20
AN21 VAXG21
AN20 VAXG22
AN18 VAXG23
AN17 VAXG24
AM24 VAXG25
AM23 VAXG26
AM22 VAXG27
AM20 VAXG28
AM18 VAXG29
AM17 VAXG30
AL24 VAXG31
AL23 VAXG32
AL21 VAXG33
AL20 VAXG34
AL18 VAXG35
AL17 VAXG36
AK24 VAXG37
AK23 VAXG38
AK21 VAXG39
AK20 VAXG40
AK18 VAXG41
AK17 VAXG42
AJ24 VAXG43
AJ23 VAXG44
AJ21 VAXG45
AJ20 VAXG46
AJ18 VAXG47
AJ17 VAXG48
AH24 VAXG49
AH23 VAXG50
AH21 VAXG51
AH20 VAXG52
AH18 VAXG53
AH17 VAXG54

SENSE
LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

1.8V RAIL

MISC

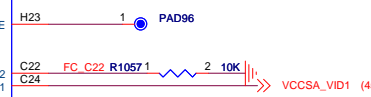
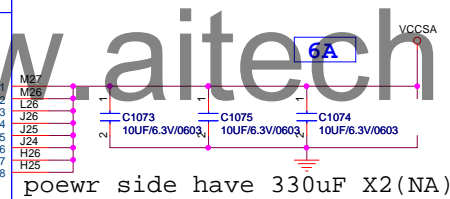
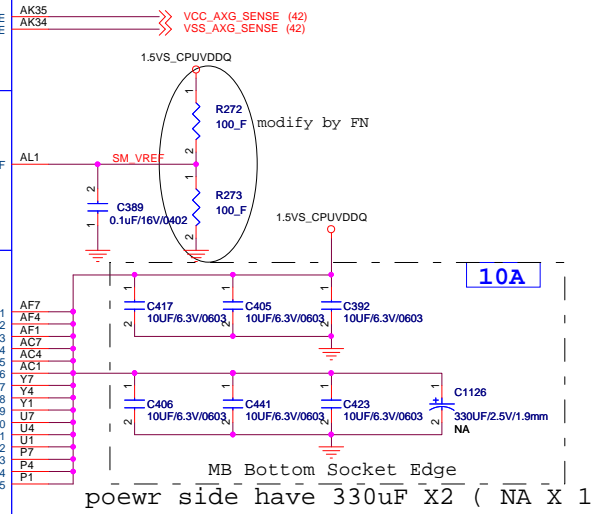
VAXG_SENSE
VSSAXG_SENSE

SM_VREF

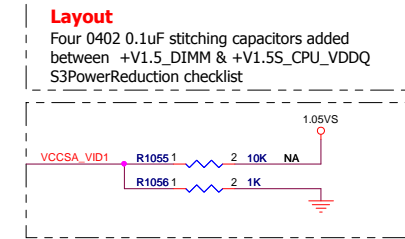
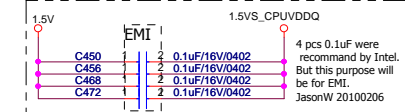
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VDDQ10
VDDQ11
VDDQ12
VDDQ13
VDDQ14
VDDQ15

VCCSA0
VCCSA1
VCCSA2
VCCSA3
VCCSA4
VCCSA5
VCCSA6
VCCSA7
VCCSA8

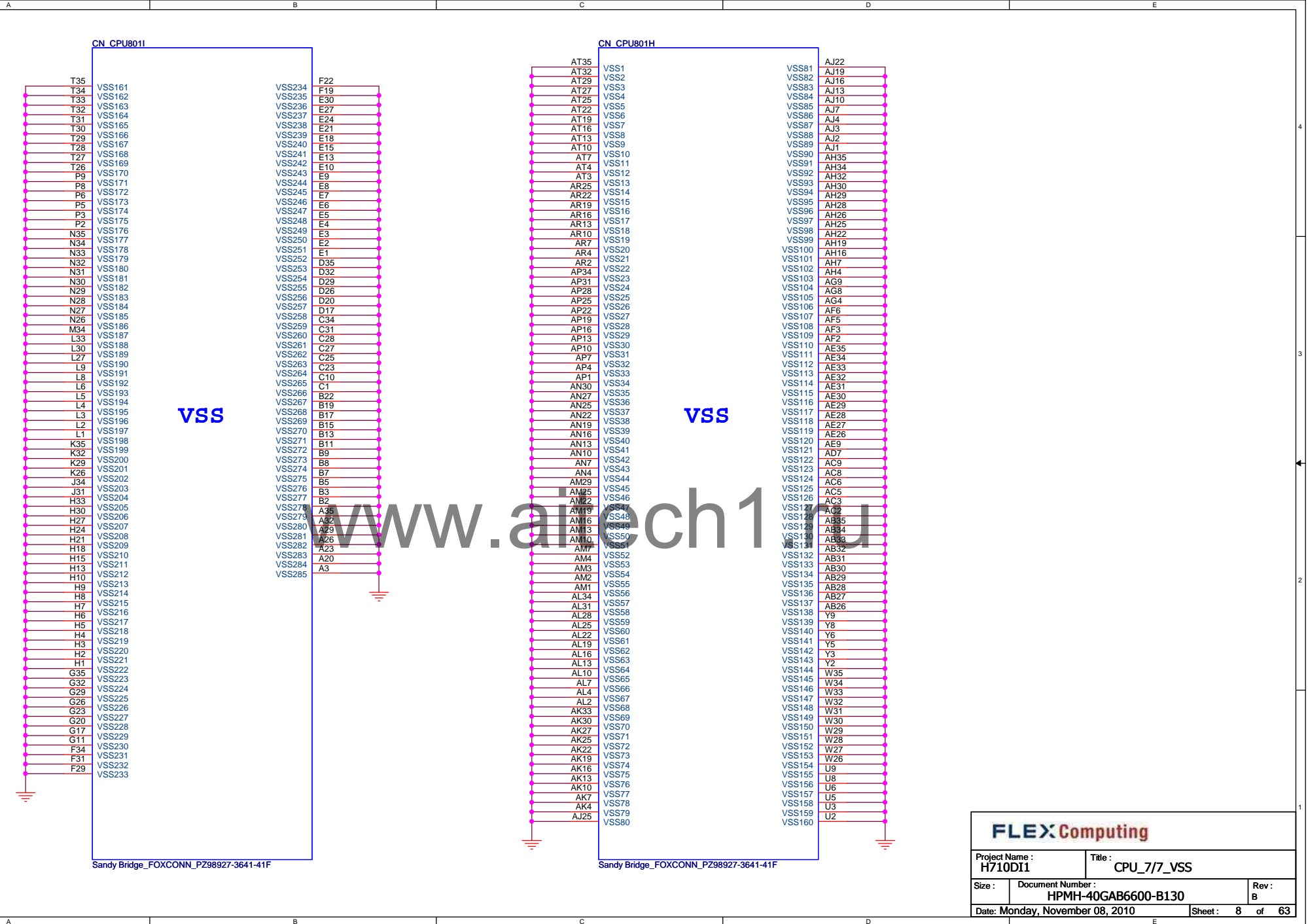
VCCSA_SENSE
FC_C22
VCCSA_VID1



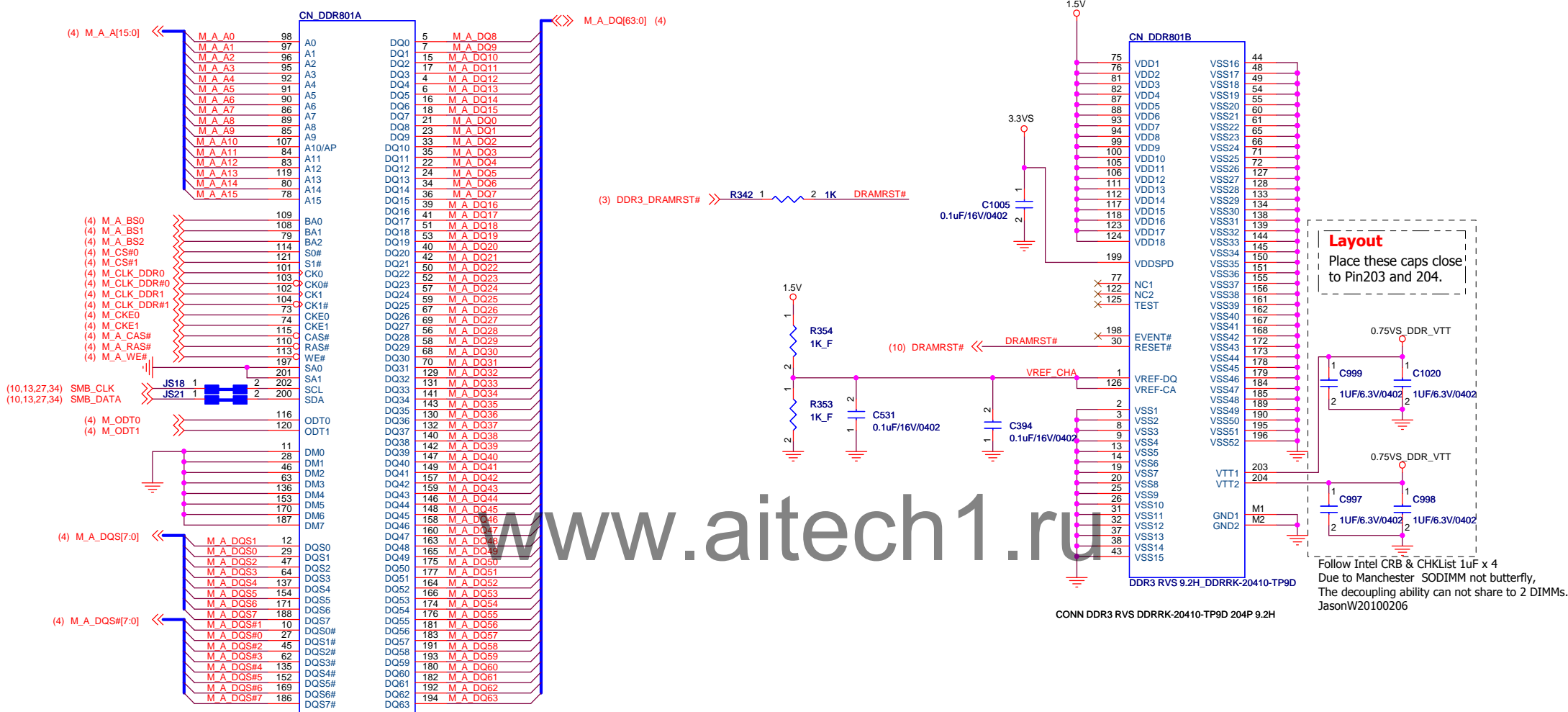
VCCSA_SEL Voltage Selection Table				
VID[0] Pin C22	VID[1] Pin C24	VCCSA Vout	2011 processor	2012 processor
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes



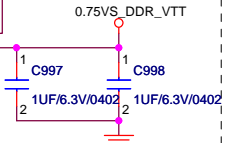
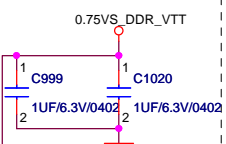
1. MB Bottom Socket Cavity 10uFX2
2. MB Bottom Socket Edge 10uFX1
3. VCCSA at processor



Channel-A



Layout
Place these caps close to Pin203 and 204.



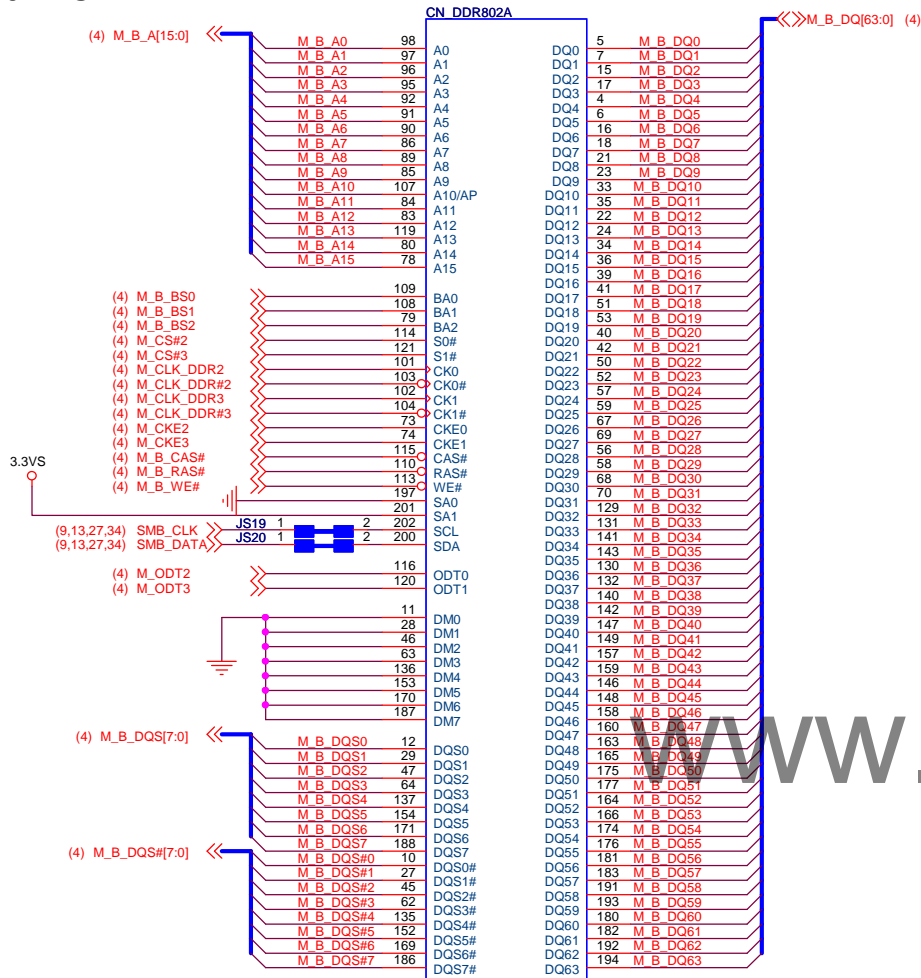
Follow Intel CRB & CHKList 1uF x 4
Due to Manchester SODIMM not butterfly,
The decoupling ability can not share to 2 DIMMs.
JasonW20100206

Layout
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM
and close to VDD Pin.

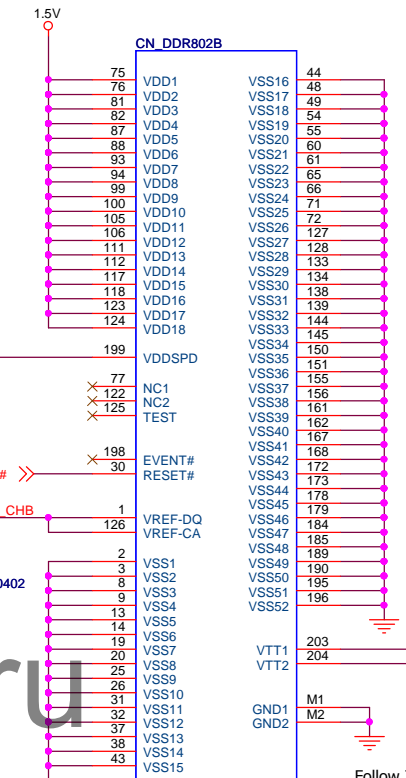
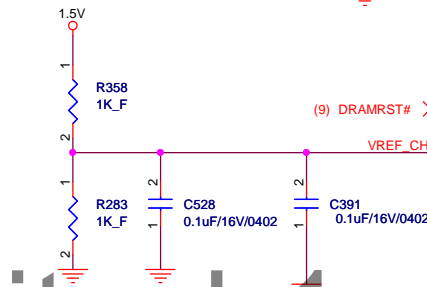
Note:
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

FLEXComputing		
Project Name :	Title :	
H710DI1	DDR3_SO-DIMM1_CHA(9H2)	
Size :	Document Number :	Rev :
	HPMH-40GAB6600-B130	B
Date: Monday, November 08, 2010		Sheet: 9 of 63

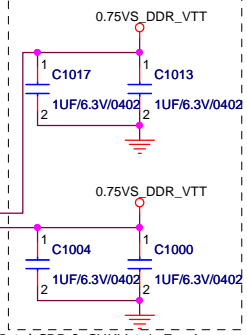
Channel-B



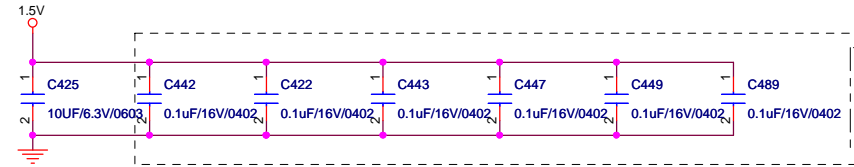
DDR3 RVS 5.2H_DDRRK-20410-TP5B
CONN DDR3 RVS DDRRK-20410-TP5B 204P 5.2H



Layout
Place these caps close to Pin203 and 204.



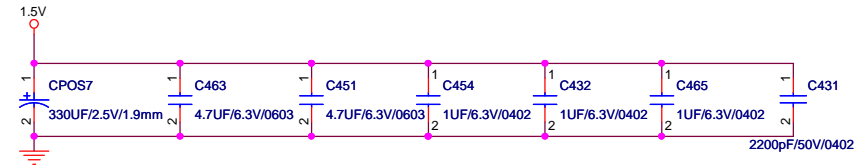
Follow Intel CRB & CHKList 1uF x 4
Due to Manchester SODIMM not butterfly,
The decoupling ability can not share to 2 DIMMs.
JasonW20100206



Layout
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM
and close to VDD Pin .

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

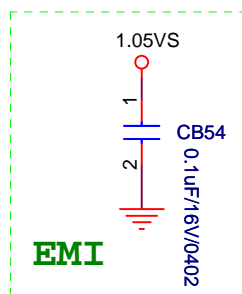
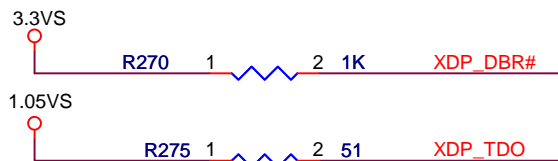
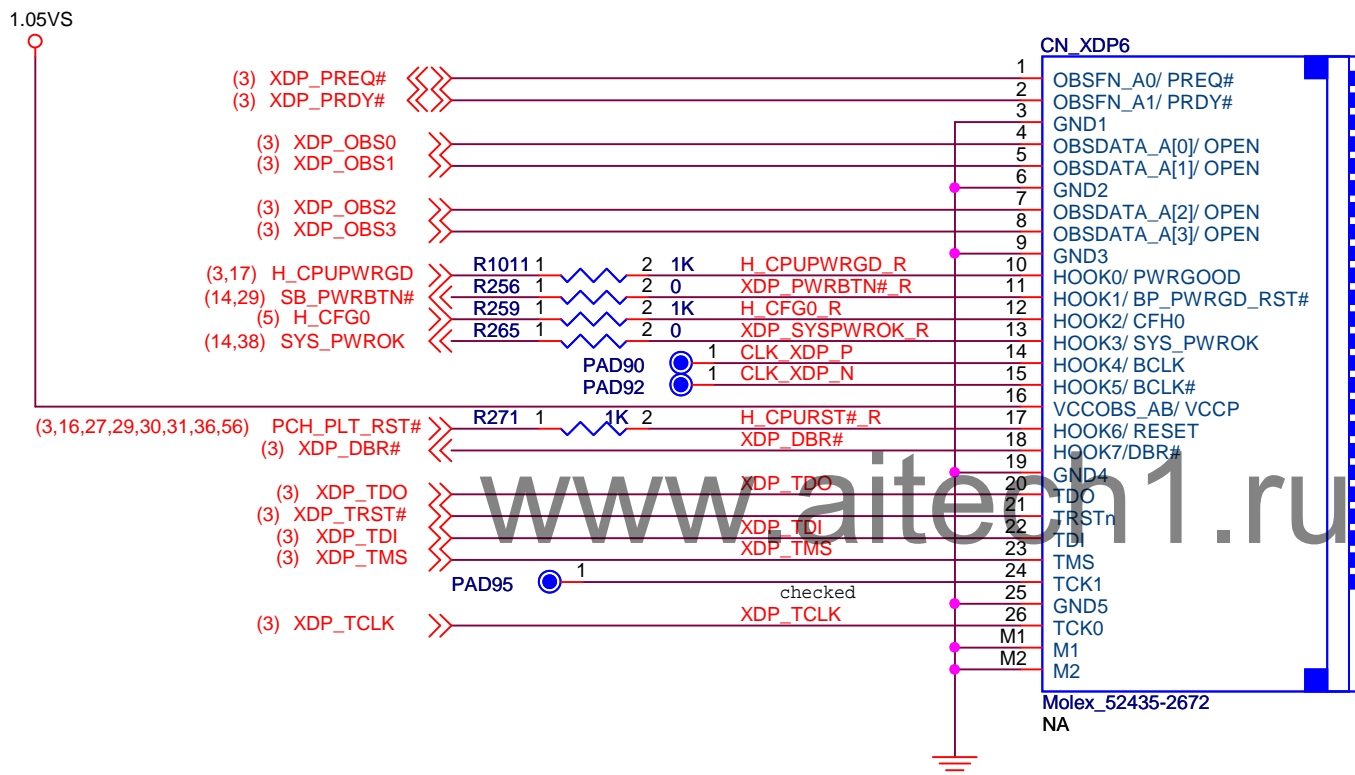
SO-DIMM Address			
SA0_DIM0 = 0, SA1_DIM0 = 0	SPD	0xA0	
	TS	0x30	
SA0_DIM1 = 0, SA1_DIM1 = 1	SPD	0xA4	
	TS	0x34	



FLEXComputing

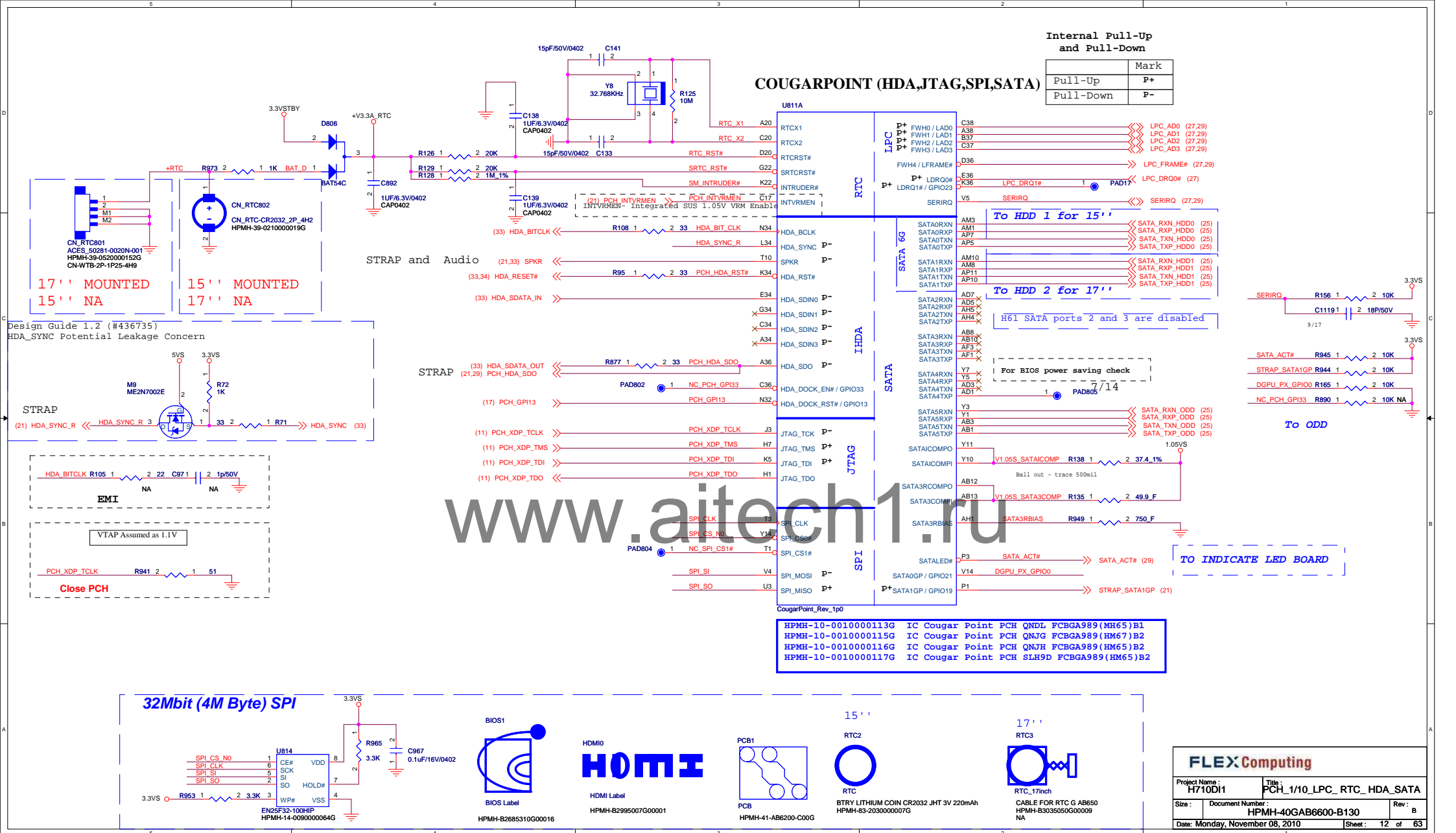
Project Name :	H710DI1	Title :	DDR3_SO-DIMM2 CHB(5H2)
Size :	Document Number :	Rev :	B
HPMH-40GAB6600-B130			
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Debug Port

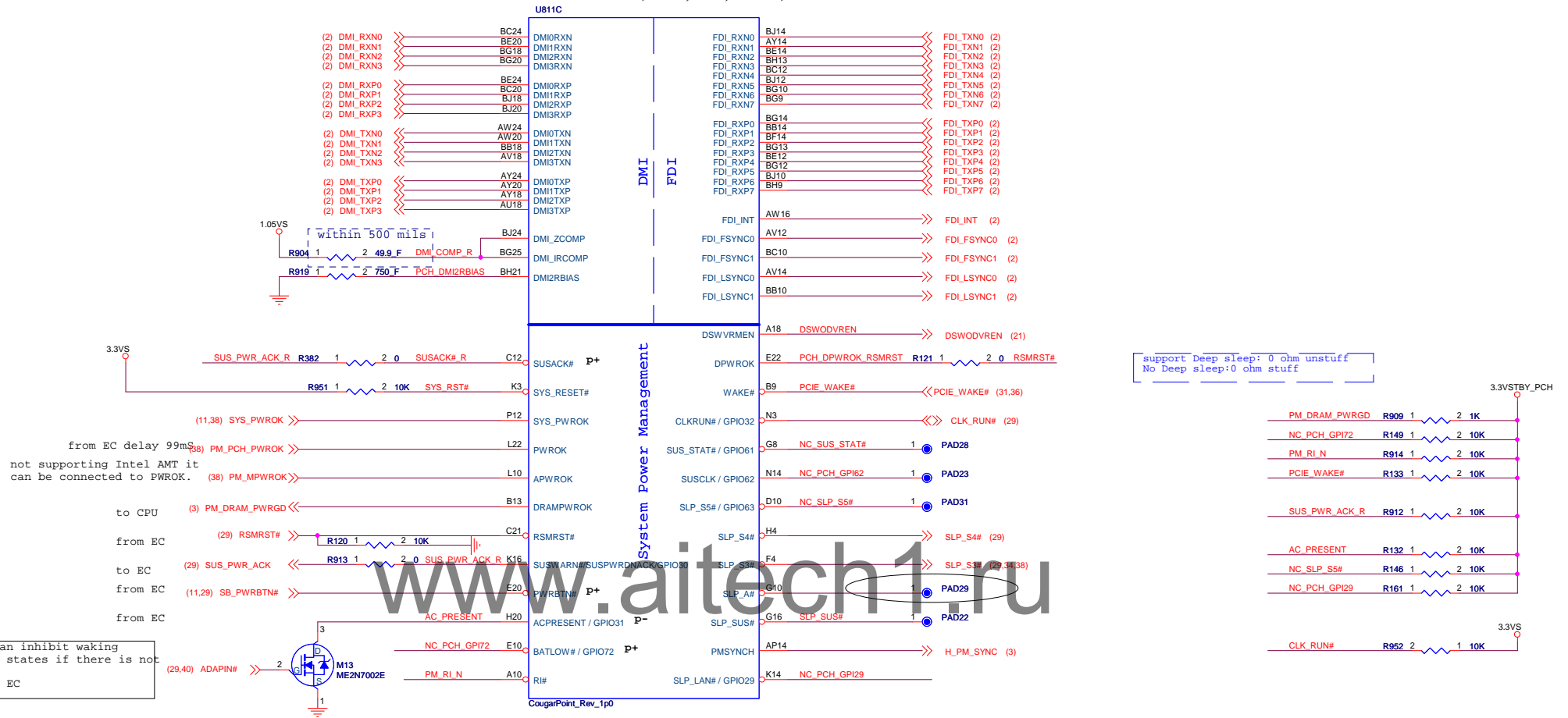


FLEX Computing

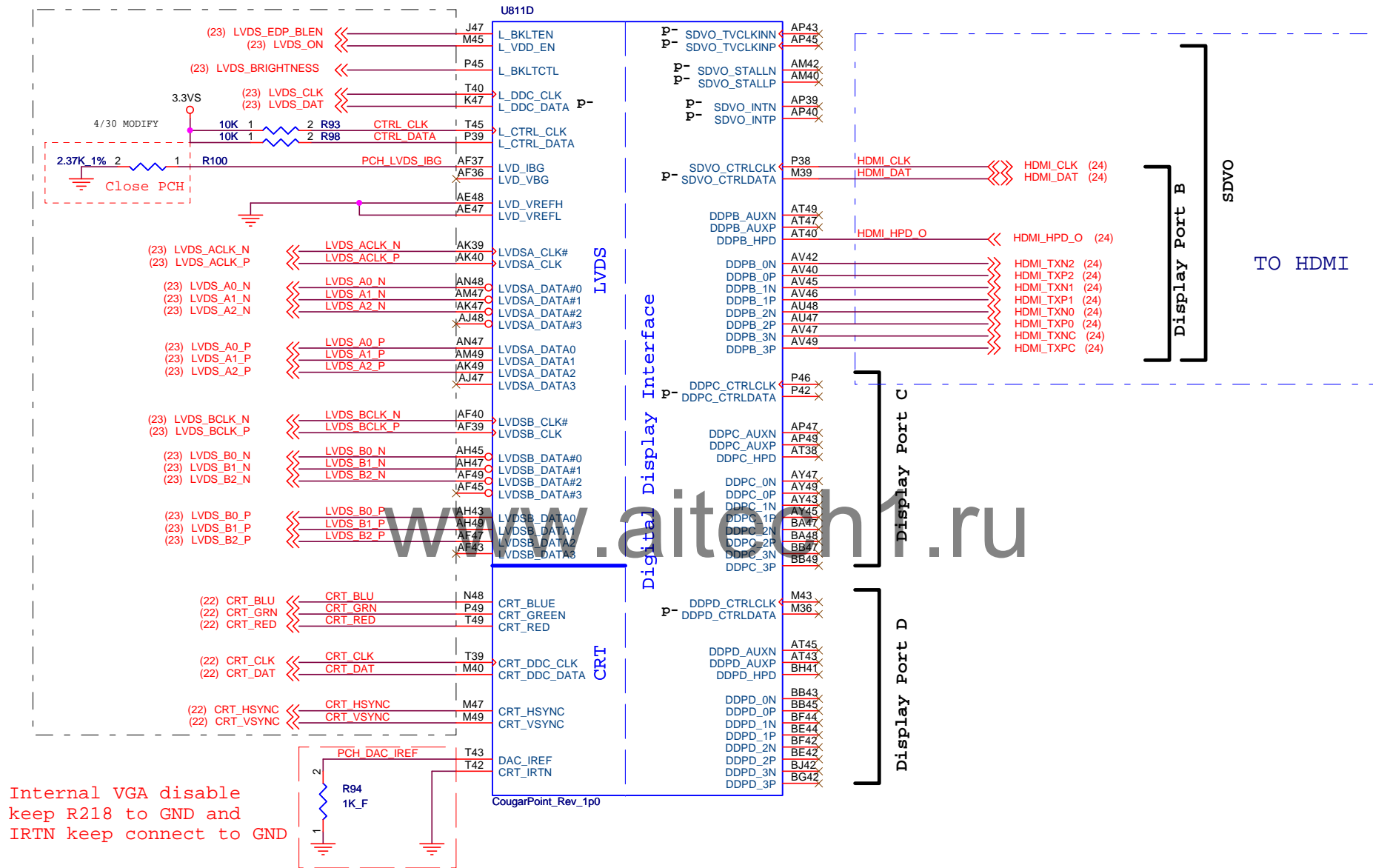
Project Name : H710DI1		Title : XDP(PROCESSOR / PCH)	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 11 of 63	



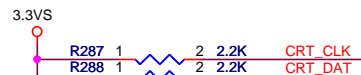
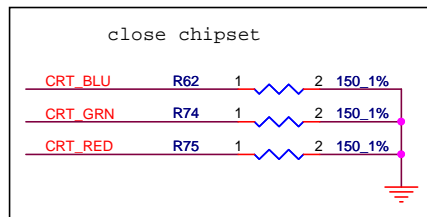
COUGARPOINT (DMI,FDI,GPIO)



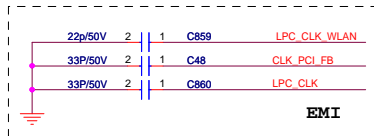
COUGARPOINT (LVDS,DDI)



Internal VGA disable
keep R218 to GND and
IRTN keep connect to GND



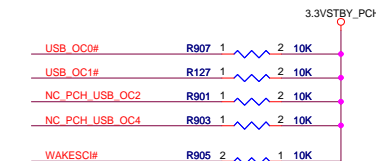
U811E		RSVD	
		RSVD1	A77
		RSVD2	A77
		RSVD3	A77
		RSVD4	B6A
		RSVD5	AT10
		RSVD6	B6B
		RSVD7	AU2
		RSVD8	A14
		RSVD9	A13
		RSVD10	A11
		RSVD11	A93
		RSVD12	A15
		RSVD13	A93
		RSVD14	A91
		RSVD15	B81
		RSVD16	B83
		RSVD17	B83
		RSVD18	B87
		RSVD19	B8B
		RSVD20	B84
		RSVD21	BFB
		RSVD22	BFB
		RSVD23	A95
		RSVD24	A91
		RSVD25	A78
		RSVD26	A95
		RSVD27	B82
		RSVD28	AT12
		RSVD29	BFB



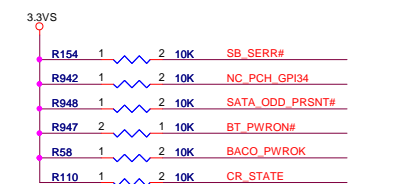
EHCI 2

DB-USB Port 0	
DB-USB Port 1	00
MB-USB Port 2	
MB-USB Port 3	00
USB-WLAN Port 4	
USB-BT Port 5	
USB-FT Port 8	
USB-WECAM Port 9	
USB-TOUCH SCREEN PORT 10	
*USB-Port1 and port9 for BIOS debug tool	

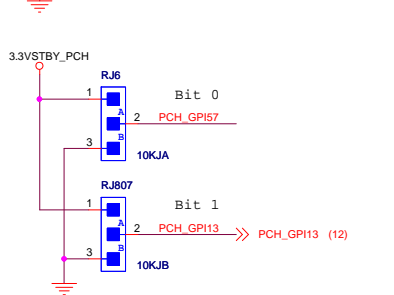
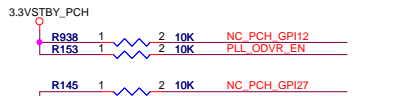
1. 14 USB ports are not available on all Standard SKU's.
2. SFF USB ports are only 12 port



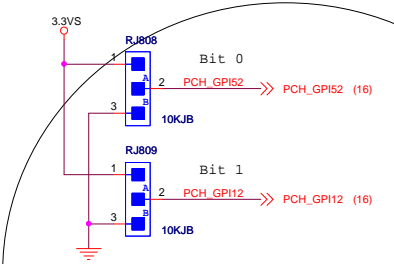
COUGARPOINT (GPIO,VSS_NCTF,RSVD)



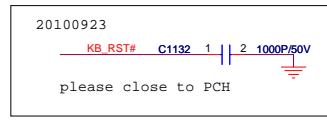
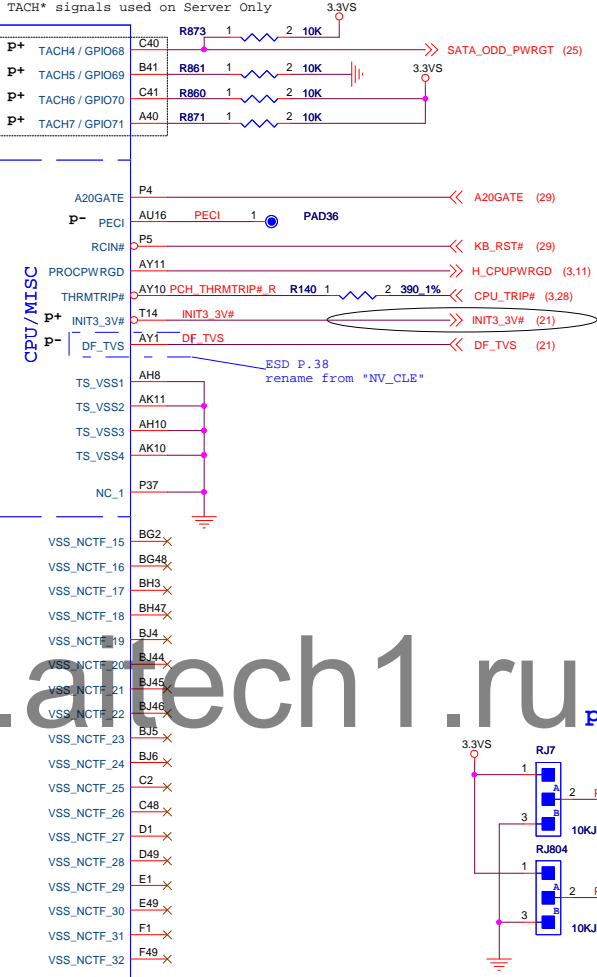
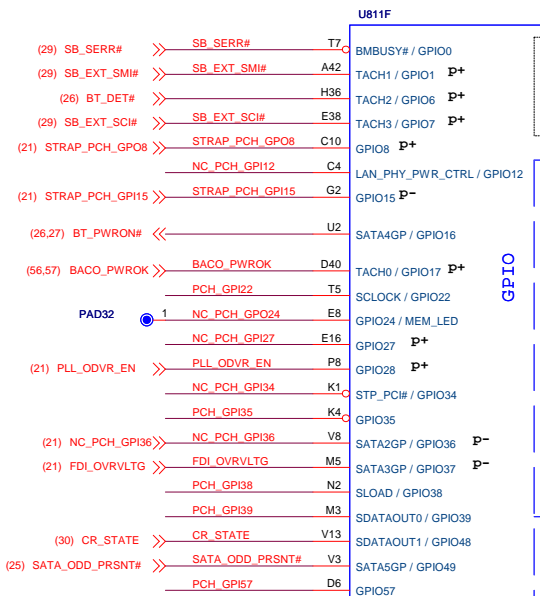
GPI048 SV_SET_UP	0ohm NA High = Strong (Default) 0ohm Mounted Low = Weak
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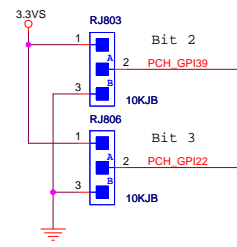
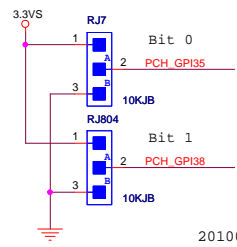
PWA rev	GPI13(RJ807)	GPI57(RJ6)
SI	0	0
PV	0	1
MV	1	0
Reserved	1	1



DC or QC HM65 or HM67	GPI12(RJ809) Bit 1	GPI52(RJ808) Bit 0
DC CPU(35W) HM65 PCH	0	0
DC CPU(35W) HM67 PCH	0	1
QC CPU(45W) HM67 PCH	1	0
QC CPU(45W) HM67 PCH	1	1



This signal has a weak internal pull-up.
Note: the internal pull-up is disabled after PLTRST# deasserts.



RJ806	RJ803	RJ804	RJ7	platform	platform ID	SI	PV
0(B)	0(B)	0(B)	0(B)	Grant 1.0 SG w/ AMD Seymour & Intel Graphic (Beats)	0x1656		
0(B)	0(B)	0(B)	1(A)	Grant 1.0 SG w/ AMD Whistler & Intel Graphic (Beats)	0x1657	SKU4	
0(B)	0(B)	1(A)	0(B)	Grant 1.0 UMA (Beats)	0x1658	SKU2	
0(B)	0(B)	1(A)	1(A)	Grant 1.0 SG w/ AMD Seymour & Intel Graphic (non Beats/Dolby)	0x3581	SKU3	
0(B)	1(A)	0(B)	0(B)	Grant 1.0 SG w/ AMD Whistler & Intel Graphic (non Beats/Dolby)	0x3582		
0(B)	1(A)	0(B)	1(A)	Grant 1.0 UMA (non Beats/Dolby)	0x3583	SKU1	
0(B)	1(A)	1(A)	0(B)	Bogart 1.0 SG w/ AMD Seymour & Intel Graphic+Subwoofer(Beats)	0x1659	SKU5,6	
0(B)	1(A)	1(A)	1(A)	Bogart 1.0 SG w/ AMD Whistler & Intel Graphic+Subwoofer(Beats)	0x165A	SKU7,8	

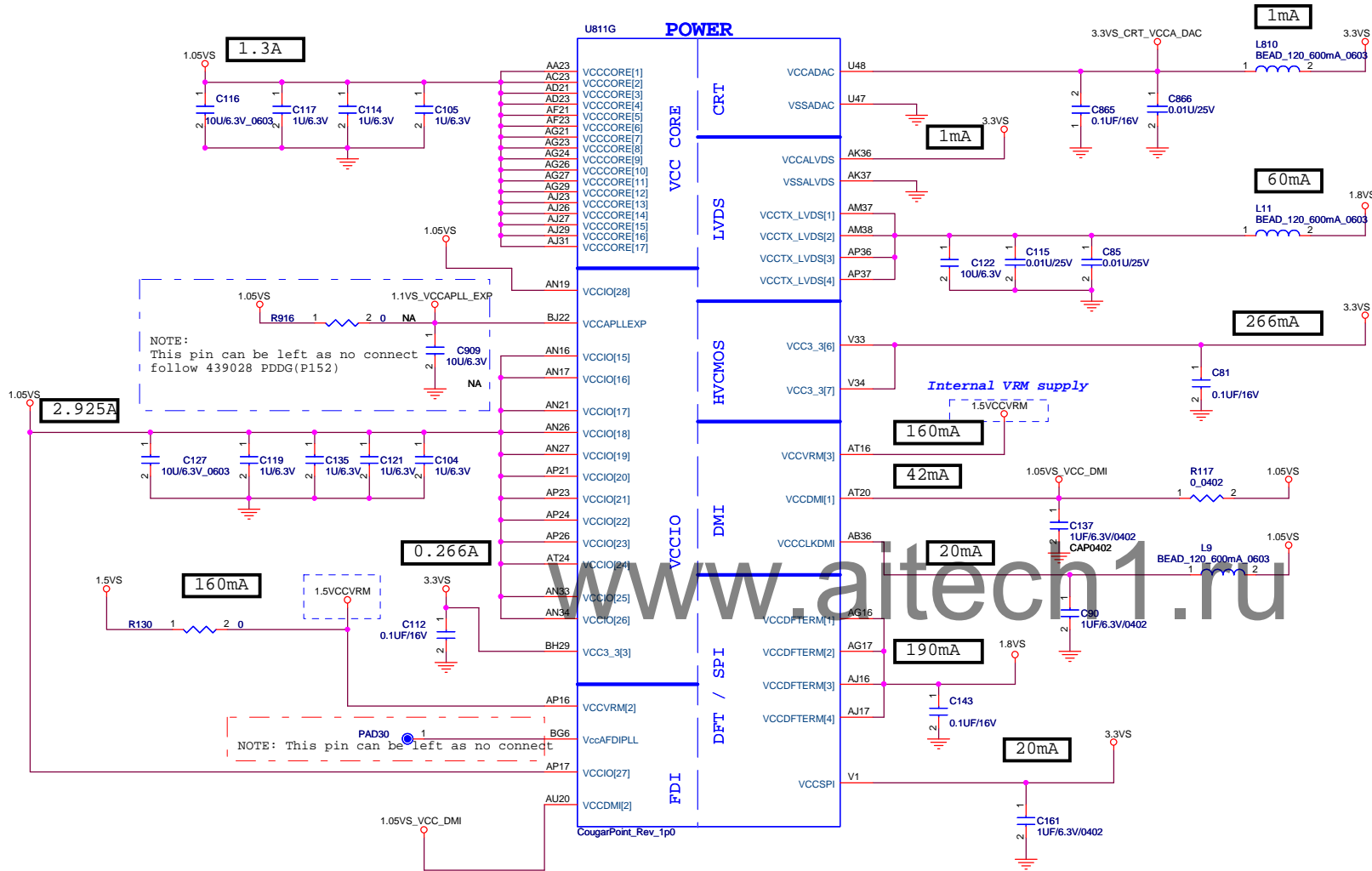
FLEX Computing

Project Name : H710D11
Title : PCH_6/10_CPU_GPIO_VSS_RSVD

Size : Document Number : HPMH-40GAB6600-B130
Date : Monday, November 08, 2010

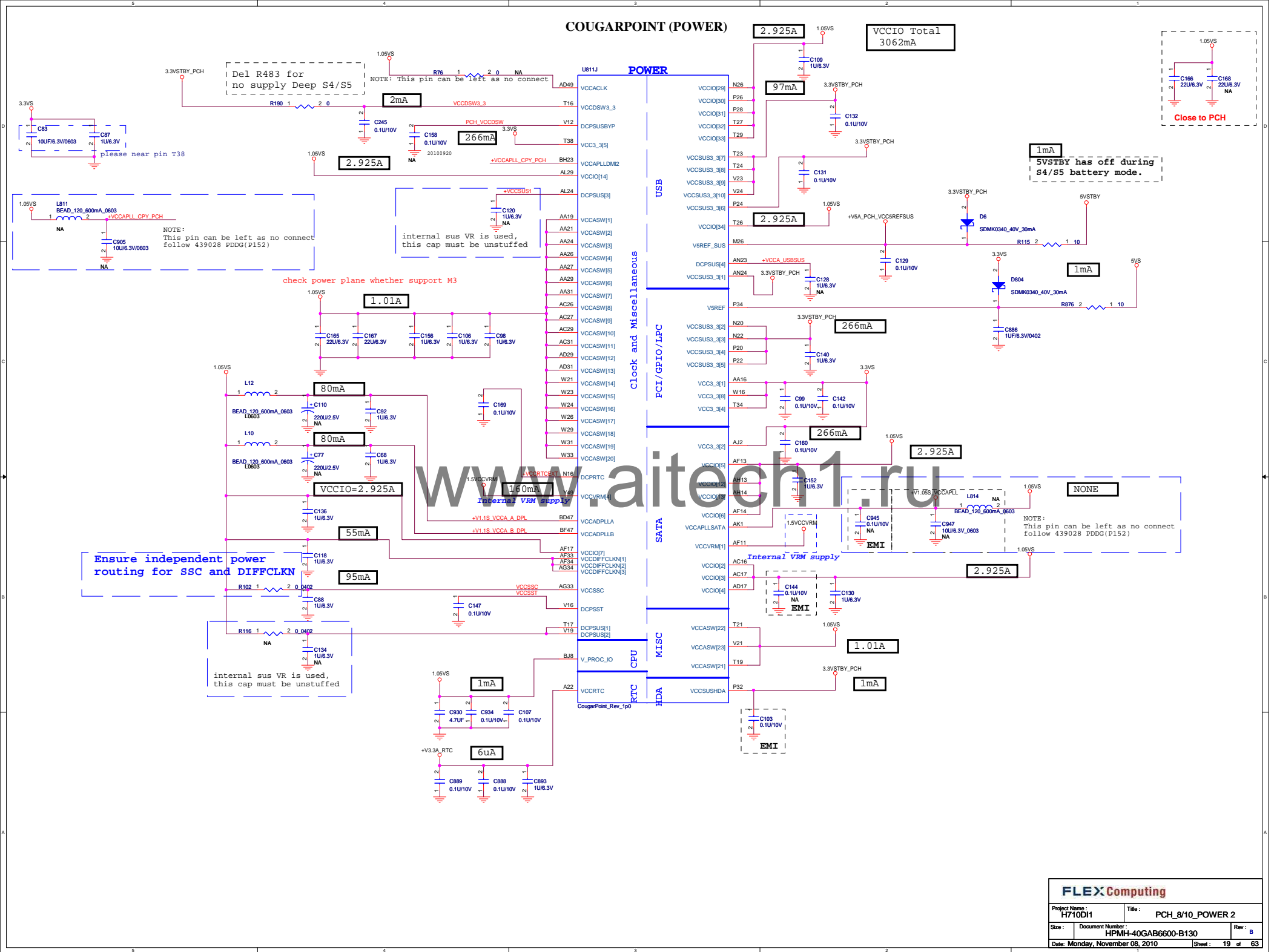
Rev : B
Sheet : 17 of 63

COUGARPOINT (POWER)



FLEX Computing		
Project Name :	H710D11	
Title :	PCH_7/10_POWER 1	
Size :	Document Number :	Rev :
	HPMH-40GAB6600-B130	B
Date: Monday, November 08, 2010	Sheet :	18 of 63

COUGARPOINT (POWER)



COUGARPOINT (GND)

U811I

U811H

H5

CougarPoint_Rev_1p0

CougarPoint_Rev_1p0

FLEX Computing		
Project Name : H710D11		Title : PCH_9/10_GND
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010		Sheet: 20 of 63

Signal	Usage	When Sampled	Internal PULL	Comment
SPKR	No Reboot	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: If the signal is sampled high, this indicates that the system is strapped to the No Reboot mode L: Cougar Point will disable the TCO Timer system reboot feature (Chipset Config Registers' Offset (3410h:Bit 5)). Default
INIT3_3V#	Reserved	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	This signal should not be pulled low
GNT[3]#/GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	H: Top Block Swap Mode disabled Default L: If the signal is sampled low, this indicates that the system is strapped to the Top Block swap mode
INTVRMEN	Integrated 1.05V VRM Enable / Disable	Always	NA	H: Integrated 1.05V VRMs enabled Default This signal should always be External pulled high L: Integrated 1.05V VRMs disabled
GNT1#/GPIO51/ BBS[1]	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	GNT1# SATA1GP Boot BIOS Location 0 0 LPC 0 1 Reserved 1 0 PCI 1 1 SPI Default
SATA1GP/ GPIO19	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	
GNT2#/GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	H: Should not be pulled low for desktop and mobile ESI compatible mode is for server platforms only. Default L: Configures DMI for ESI compatible operation
HDA_SDO	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of RSMRST#	Internal PD	H: If sampled high, the Flash Descriptor Security will be overridden. L: If strap is sampled low, (Default) the security measures defined in the Flash Descriptor will be in effect. This signal should not be pulled high
DF_TVS	DMI and FDI Tx/ Rx Termination Voltage	Rising edge of PWROK	Internal PD	The internal pull-down is disabled after PLTRST# deasserts
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	Internal PU	H: The On-Die PLL voltage regulator is enabled when sampled high Default L: When sampled low the On-Die PLL Voltage Regulator is disabled
HDA_SYNC	On-Die PLL Voltage Regulator Select	Rising edge of RSMRST# pin	Internal PD	H: On-Die PLL VR is supplied by 1.5 V Default L: On-Die PLL VR is supplied by 1.8 V
GPIO15	TLS Confidentiality	Rising edge of RSMRST# pin	Internal PD The weak internal pull-down is disabled after RSMRST# deasserts	H: Intel ME Crypto TLS cipher suite with confidentiality Default L: Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
L_DDC_DATA	LVDS Detected	Rising edge of PWROK	Internal PD The internal pull-down is disabled after PLTRST# deasserts.	H: LVDS is detected Default L: LVDS is not detected
SDVO_CTLRDATA	Port B Detected	Rising Edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port B is detected L: Port B is not detected Default
DDPC_CTLRDATA	Port C Detected	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port C is detected L: Port C is not detected Default
DDPD_CTLRDATA	Port D Detected	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port D is detected L: Port D is not detected Default
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	Always	NA	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
SATA2GP/ GPIO36	Reserved	Rising edge of PWROK	Internal PD (The internal pull-down is disabled after PLTRST# deasserts.)	NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved	Rising edge of PWROK	Internal PD (The internal pull-down is disabled after PLTRST# deasserts.)	NOTE: NOTE: This signal should not be pulled high when strap is sampled.
GPIO8	Reserved	Rising edge of RSMRST#	Internal PU (Pull-up is disabled after RSMRST# is deasserted.)	NOTE: This signal should not be pulled low

PAD24 1 SPKR (12,33)

PAD21 1 INIT3_3V# (17)

R70 1 2 1K NA STRAP_GNT3# (16)

+V3.3A_RTC
R896 1 2 330K PCH_INVRMEN (12)

R69 1K NA R943 1K NA
STRAP_GNT1# (16)
STRAP_SATA1GP (12)

PAD10 1 STRAP_GNT2# (16)

3.3VS
R1115 1 2 1K NA PCH_HDA_SDO (12,29)

1.8VS
R933 1 2 2.2K
(3) H_SNB_IVB# R929 1 2 1K DF_TVS (17)
PLACE 2.2K CLOSE TO THE BRANCHING POINT

PAD35 1 PLL_ODVR_EN (17)

3.3VSTBY_PCH
R147 1 2 1K HDA_SYNC_R (12)

3.3VSTBY_PCH
R939 1 2 1K STRAP_PCH_GPI15 (17)

+V3.3A_RTC
R1067 1 2 330K
R899 1 2 330K NA DSWODVRN (14)
DSWODVRN

R1110 1 2 10K NC_PCH_GPI36 (17)

R151 1 2 10K FDI_OVRVLGT (17)
FDI_OVRVLGT

R918 1 2 1K STRAP_PCH_GPO8 (17)

NO REBOOT	
NA	Low=Disable(Default)
MOUNTED	High=Enable

A16 swap override Strap	
STP_A16OVR	Low = A16 swap override High = Default

INTVRMEN= Integrated SUS 1.05V VRM Enable

Flash Descriptor Security Override	
PCH_HDA_SDO	NA Low=Disable(Default) MOUNTED High=Enable

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

PLL ON DIE VR ENABLE	
PLL_ODVR_EN	ENABLE- UNSTUFF DISABLE-STUFF

HR only support 1.5 V
HDA_SYNC need PU to HDA SUS rail through 1k ohm
for 451710_451710 SPEC

DSWODVRN - On Die DSW VR Enable	
Pull High	Enable (Default)
Pull Down	Disable

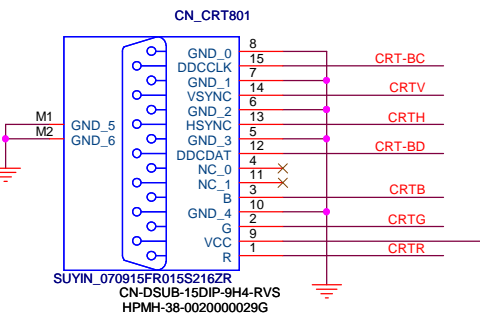
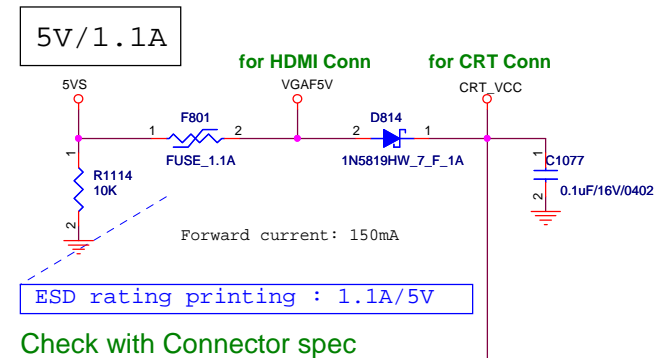
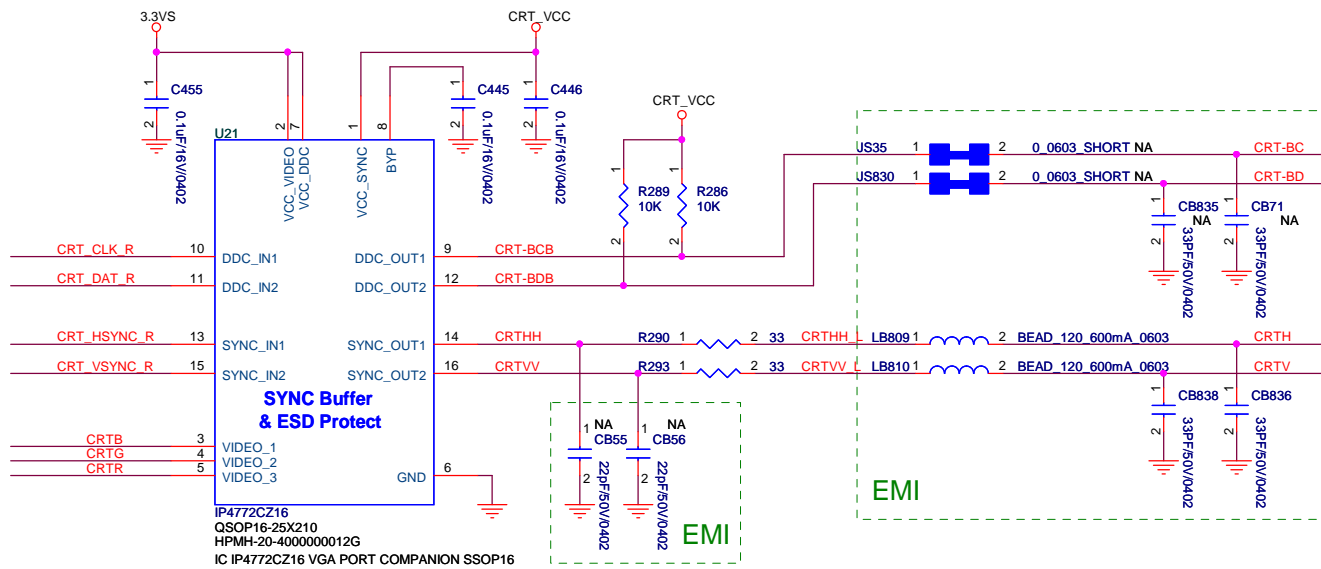
DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLGT)	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

GPIO8 Integrated Clock Chip Enable	
High	Disable
Low	Enable(default)

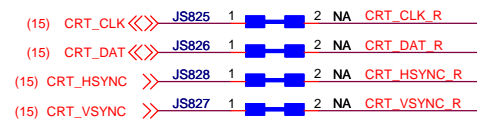
FLEXComputing			
Project Name : H710D11		Title : PCH_10/10_STRAP	
Size :	Document Number : HPMH-40GAB6600-B130	Rev :	B
Date: Monday, November 08, 2010		Sheet: 21 of 63	

D-Sub

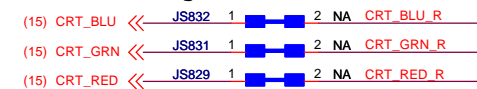


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For DGPU debug



For DGPU debug



FLEXComputing

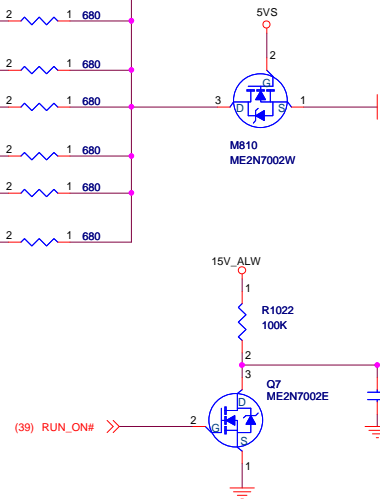
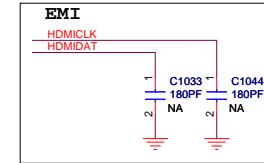
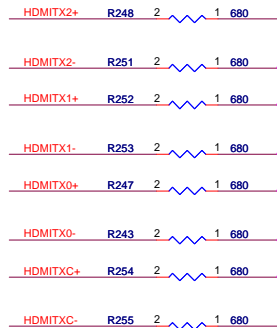
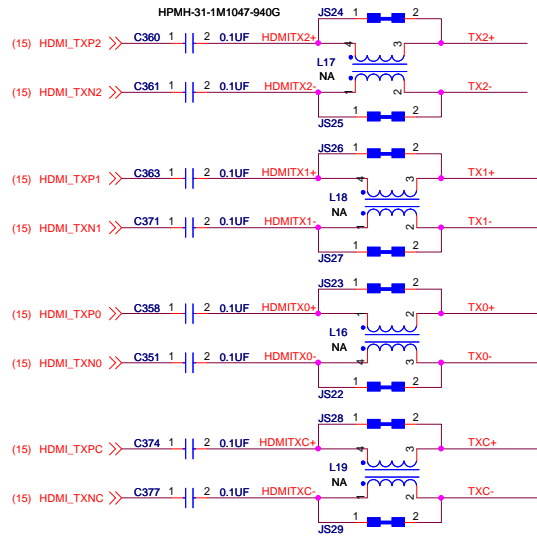
Project Name :	H710D11	Title :	CRT CONN
Size :	Document Number :	Rev :	B
Date :	Monday, November 08, 2010	Sheet :	22 of 63

HDMI

CLOSE to CN_HDMI1

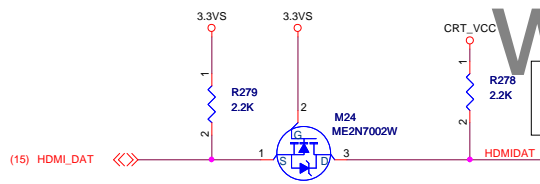
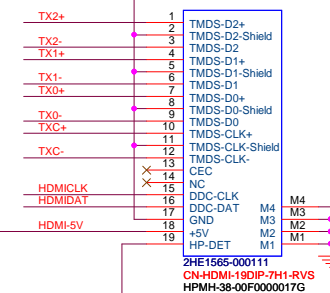
HPMH-32-4000000104G

Intel Huron River: 680 ohm
AMD Danube: 715 ohm
AMD Sabine: 715 ohm

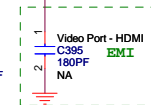
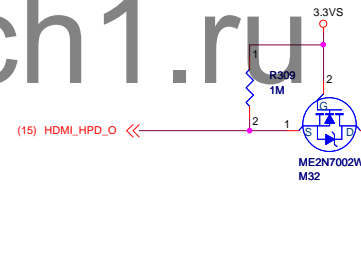
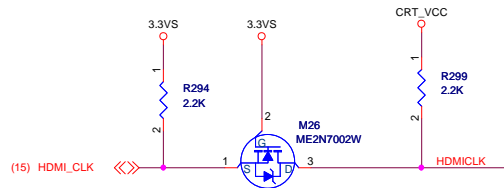


HDMI

CN_HDMI801



HDMI test
C1 -- Cp=45pf
C2 -- Cp=46pf (spec<50pf)

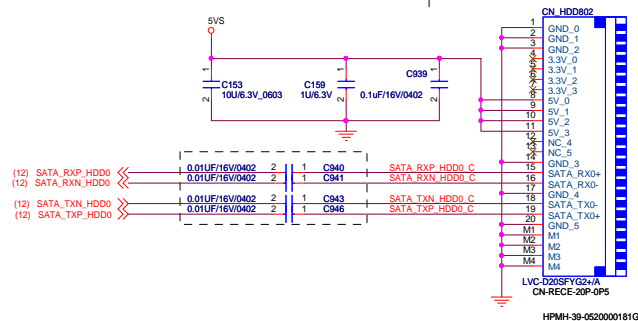


FLEX Computing

Project Name : H710DI1		Title : HDMI CONN	
Size : Custom	Document Number : HPMH-40GAB6600-B130		Rev : B
Date : Monday, November 08, 2010		Sheet : 24 of 63	

HDD

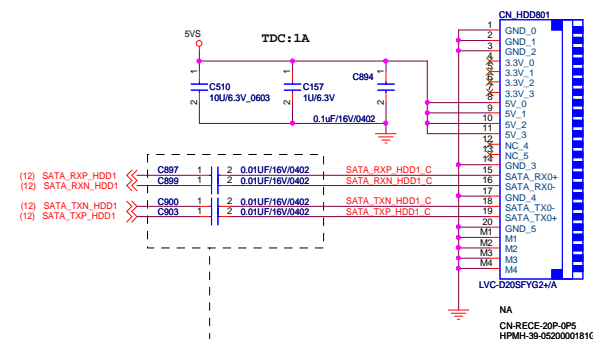
Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist



2nd HDD

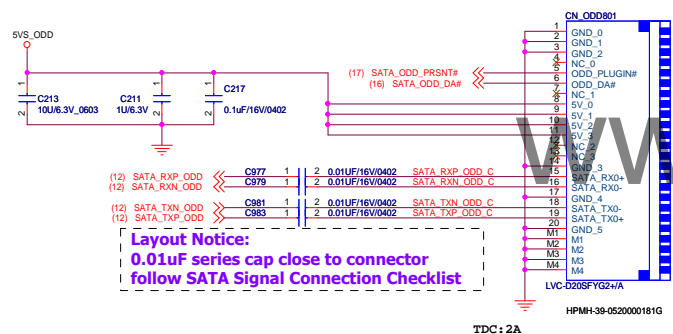
FOR 17" MB USE WTB CONNECTOR

CONN SPEC: 0.3A/PIN



Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist

ODD



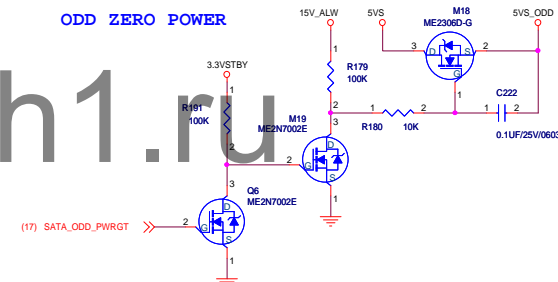
Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist

TDC: 2A

Change to Cable type Conn

ODD Zero Power

Check if meet max current!!



G-Sensor

G-SENSOR

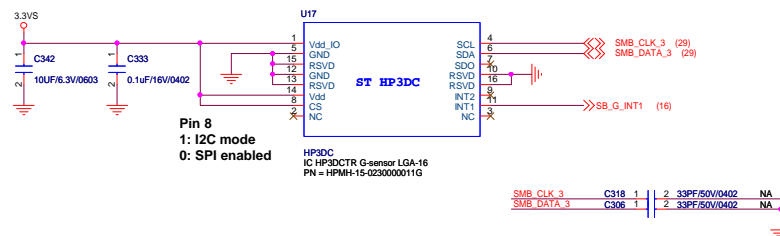
ST HP3DC

3.3VS

ADDR: 0011000x(30h) - SDO PD

ADDR: 0011010x(32h) - SDO NC

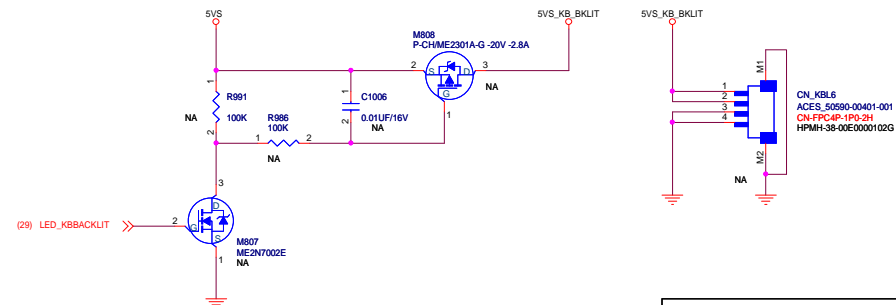
SINK: ??mA@VoL=0.33V(MAX)



Pin 8
1: I2C mode
0: SPI enabled

HP3DC
IC HP3DCTR G-sensor LGA-16
PN = HPMH-15-023000011G

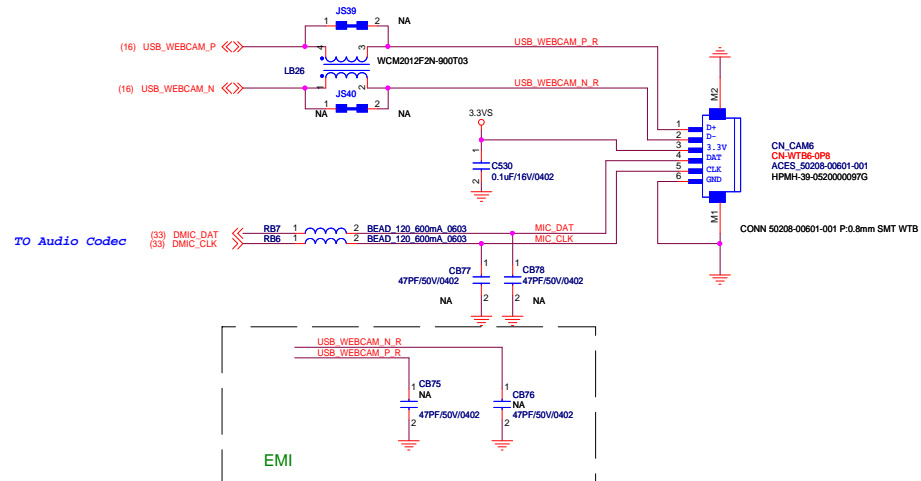
KB Backlit



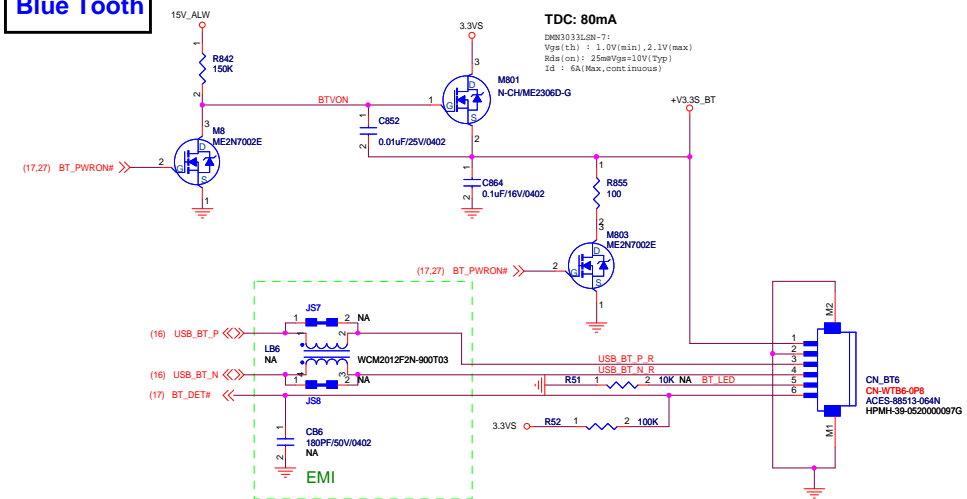
FLEX Computing

Project Name:	H710D11	Title:	HDD_ODD_G-Sensor_KB BKL
Size:	Document Number:	HPMH-40GAB6600-B130	Rev: B
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Web CAM



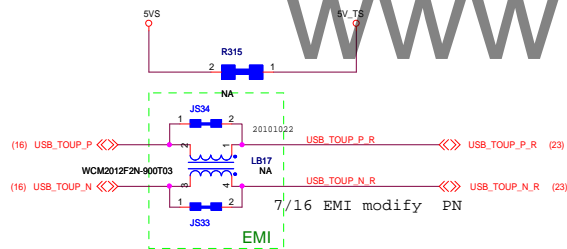
Blue Tooth



TouchScreen (Module CONN)

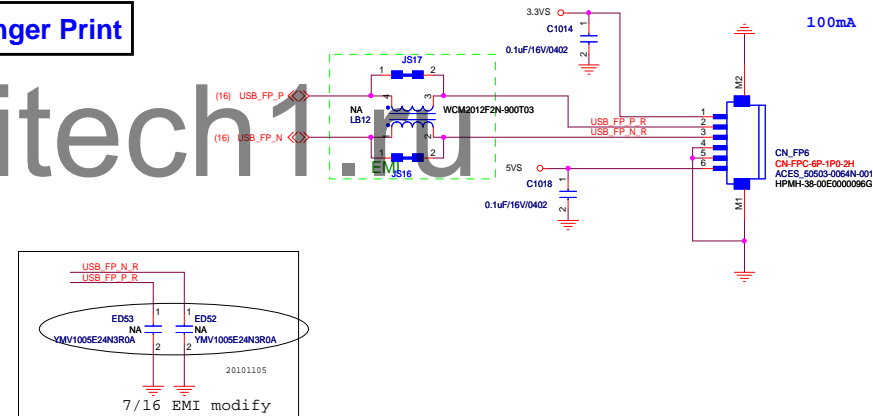
Touch Screen power is 5V type

Peak 200mW 40mA

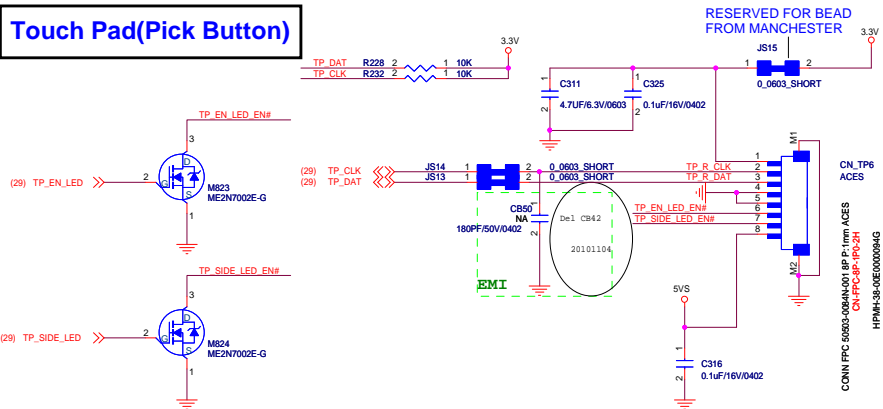


15.6" MOUNT
17.3" NA

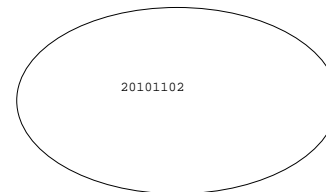
Finger Print



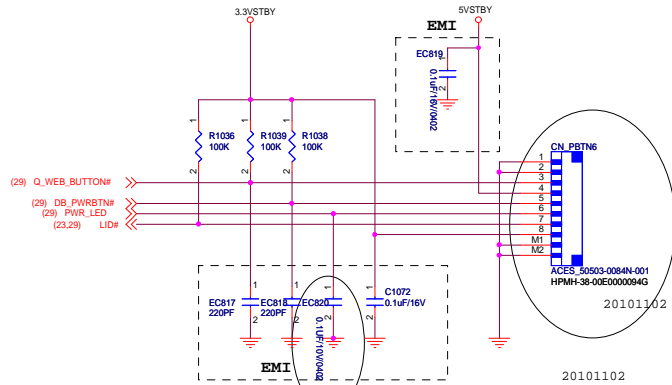
Touch Pad(Pick Button)



LID

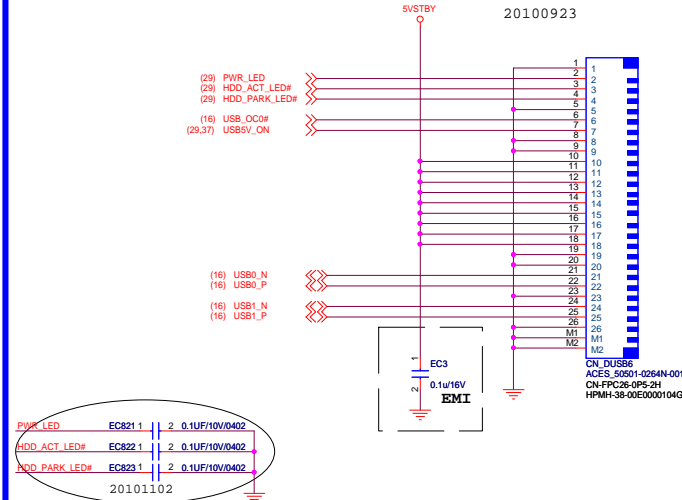


PWRBTN BOARD

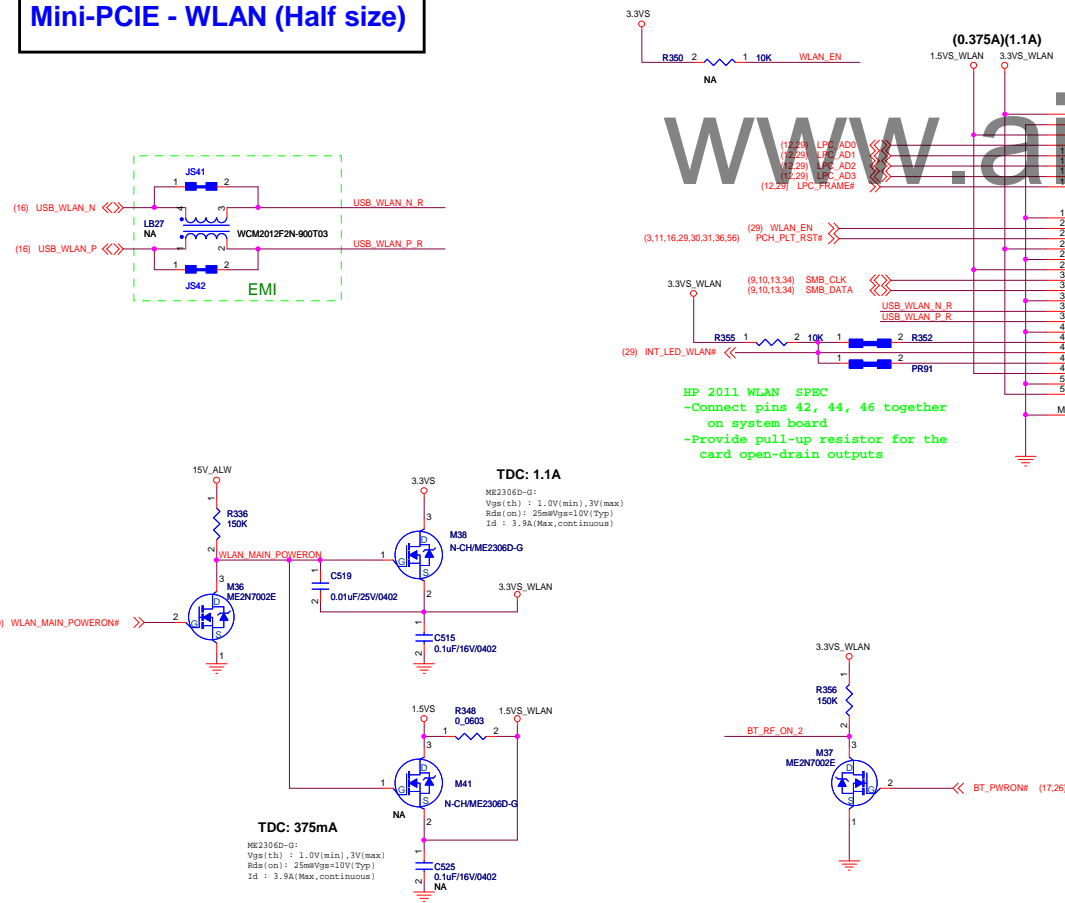


connector on Mother Board for
Power Button/LED/LID Daughter board

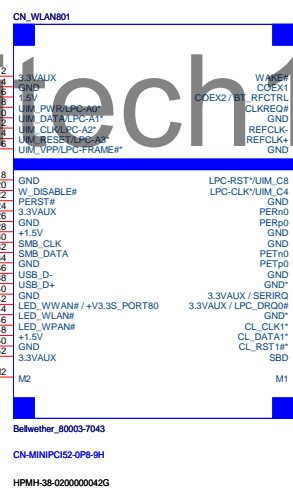
USB BOARD



Mini-PCIE - WLAN (Half size)

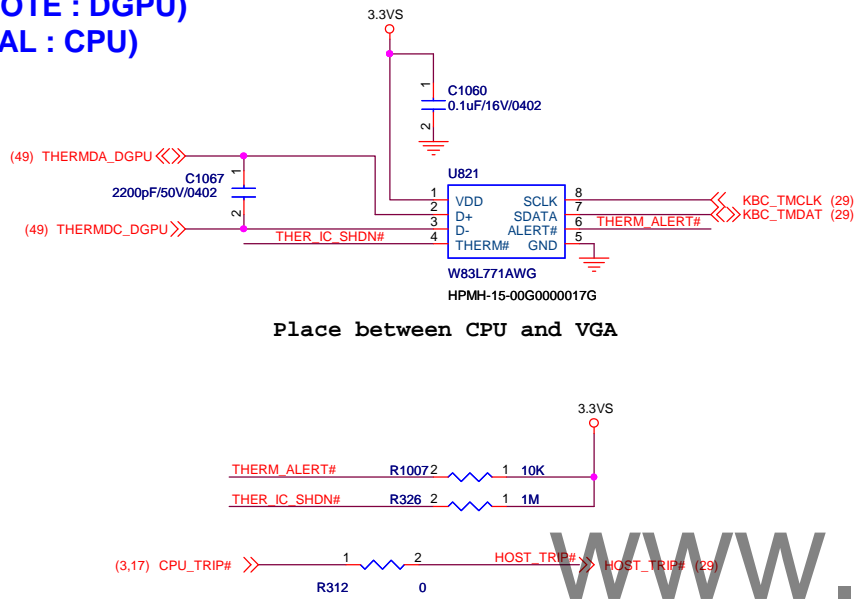


WLAN CONNECTOR

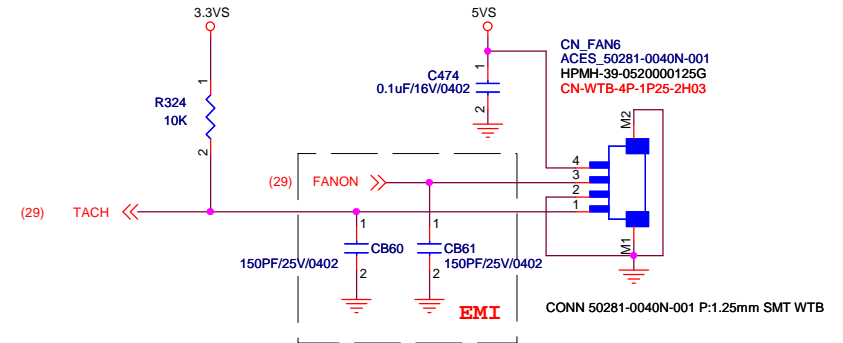


HP 2011 WLAN SPEC 2nd RF ON/OFF Pin
Primary path is to implement it on pin 51,
but 0 Ohm strap to pin 19 required for
Intel Rainbow Peak ES2 cards use
(QS will transition to pin 51).

**Thermal Sensor
(REMOTE : DGPU)
(LOCAL : CPU)**



FAN CONN

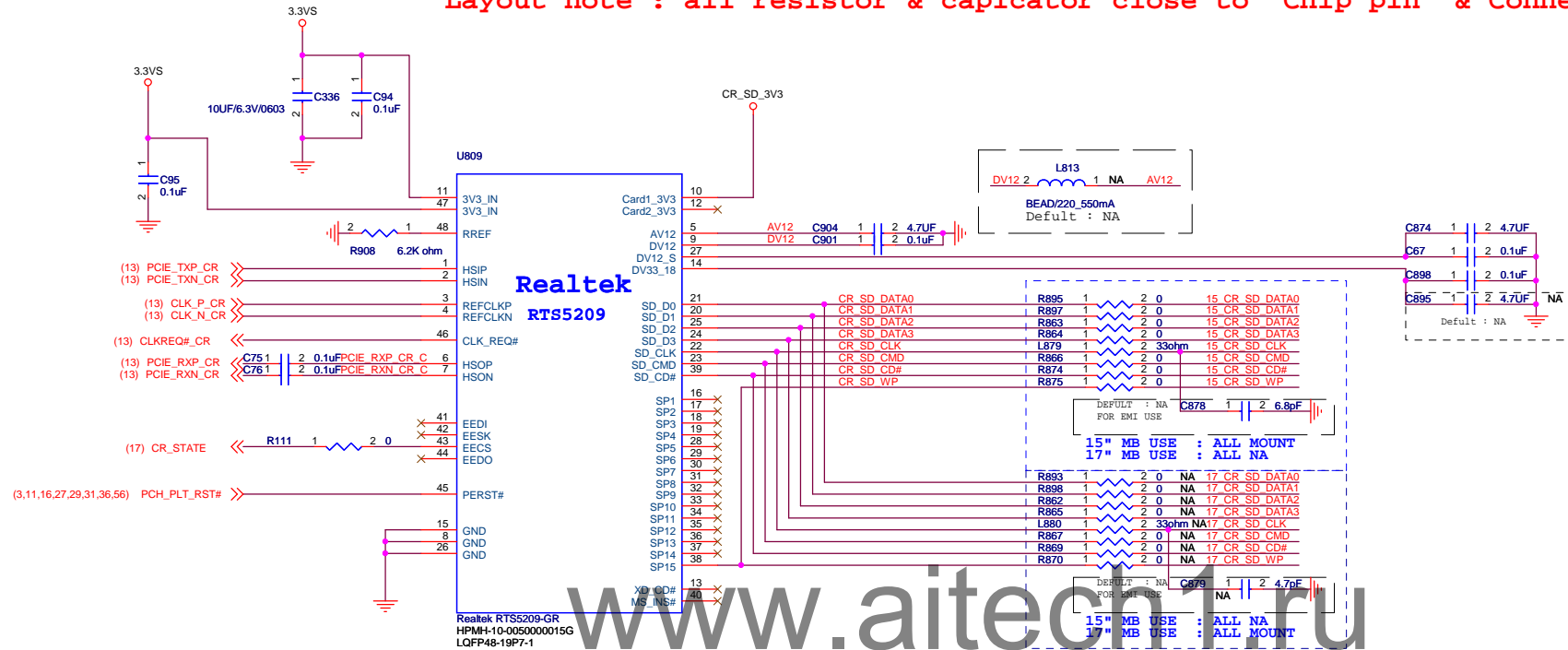


THERMAL IC FOR CPU or DGPU

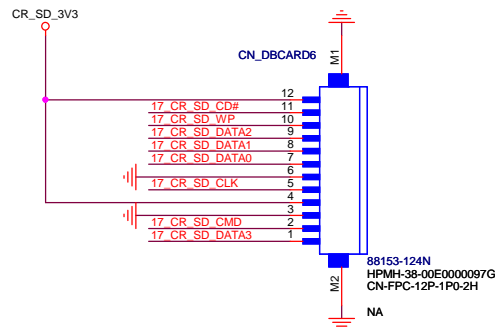
WINBOND	W83L771AWG	ODMH-15-00G0000017G 1001100x(98h)
ON SEMI	ADT7421ARMZ-REEL	???
GMT	G780P81U	???

Card Reader

Layout note : all resistor & capicator close to Chip pin & Connector pin

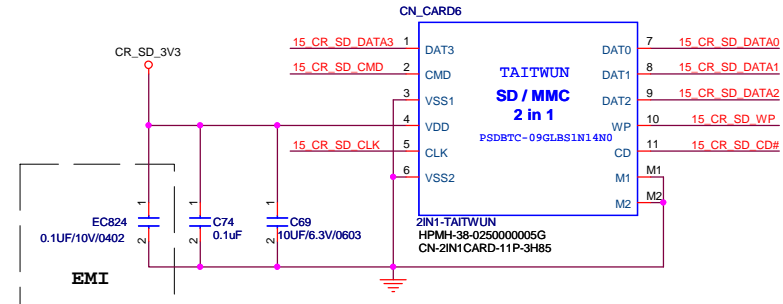


FOR 17" MB USE WTB CONNECTOR



FOR 15" MB ALL COMPONENT : NA
FOR 17" MB ALL COMPONENT : MOUNT

FOR 15" MB USE CardReader CONNECTOR



FOR 15" MB ALL COMPONENT : MOUNT
FOR 17" MB ALL COMPONENT : NA

FLEX Computing

Project Name : H710DI1		Title : Card Reader (R5U220)	
Size :	Document Number :	HPMH-40GAB6600-B130	
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Gbit LAN Controller

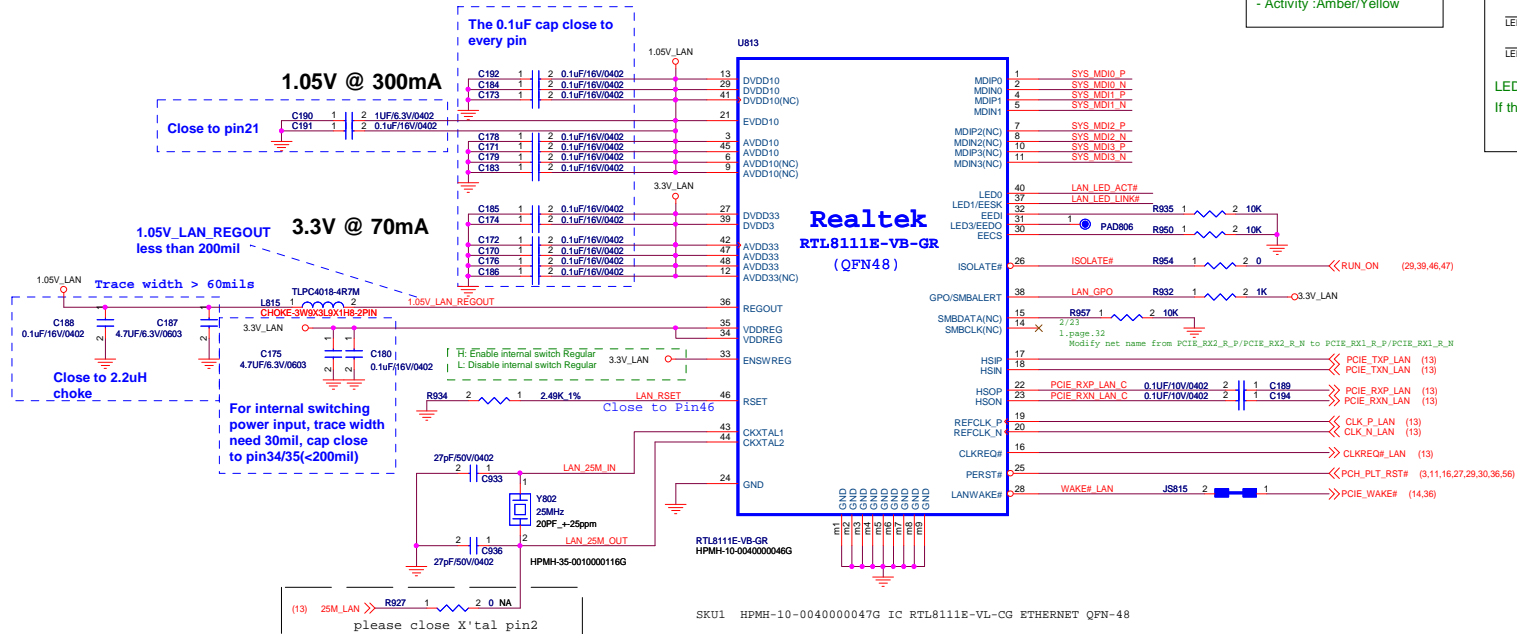
Mini-spec requirements:

- 10/100/1000 :
- Link :White
- Activity :Amber/Yellow

RTL8111E

LEDS1-0	00	01	10	11
LED0	ACT ALL	LINK ALL	LINK10	LINK10
	/ACT ALL	/ACT ALL	/ACT10	/ACT10
LED1	LINK100	LINK100	LINK100	LINK100
				/ACT100
LED3	LINK1000	LINK1000	LINK1000	LINK1000
				/ACT1000

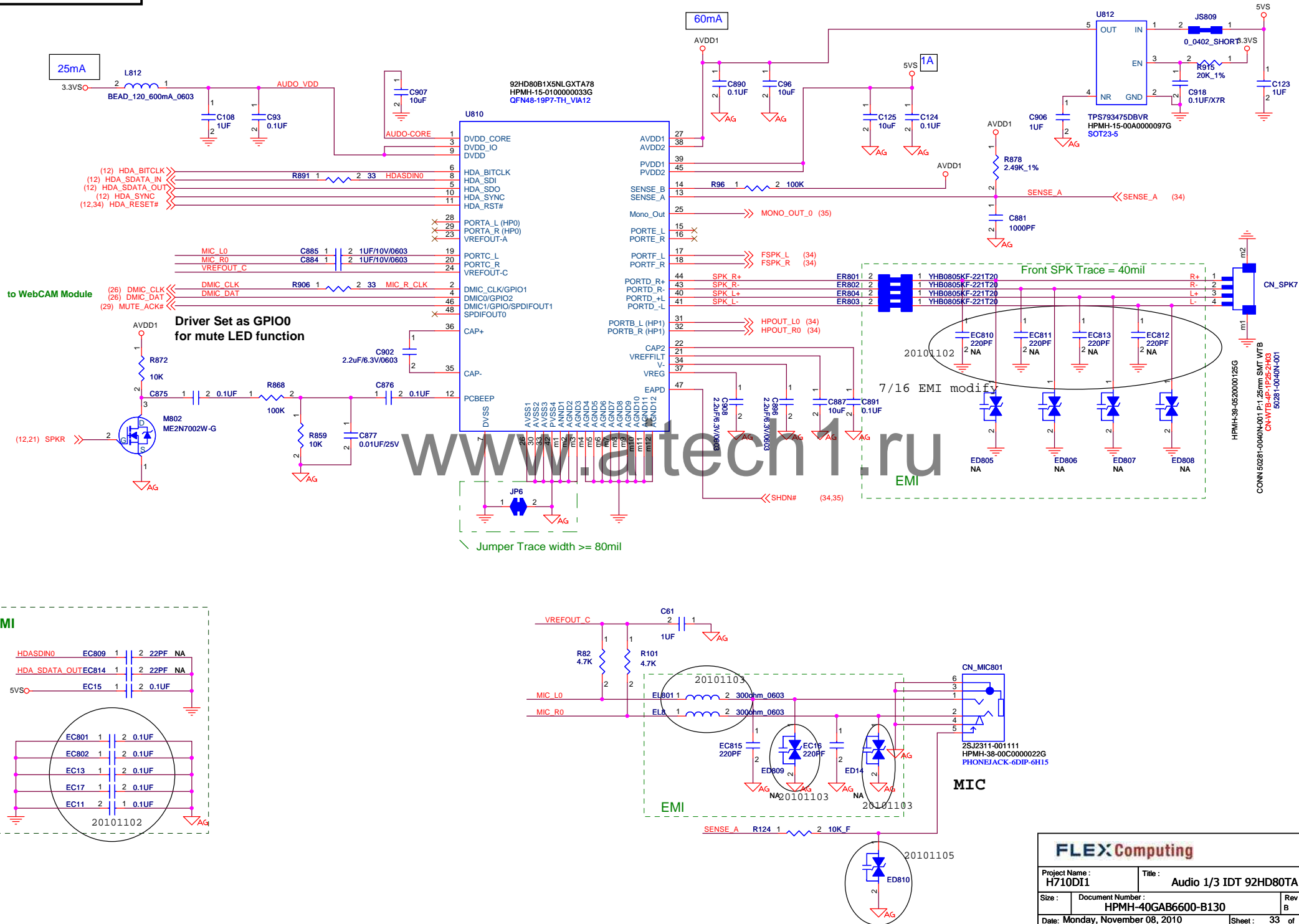
LEDS1-0s initial value comes from the EEPROM
If there is no EEPROM, the default value is 11



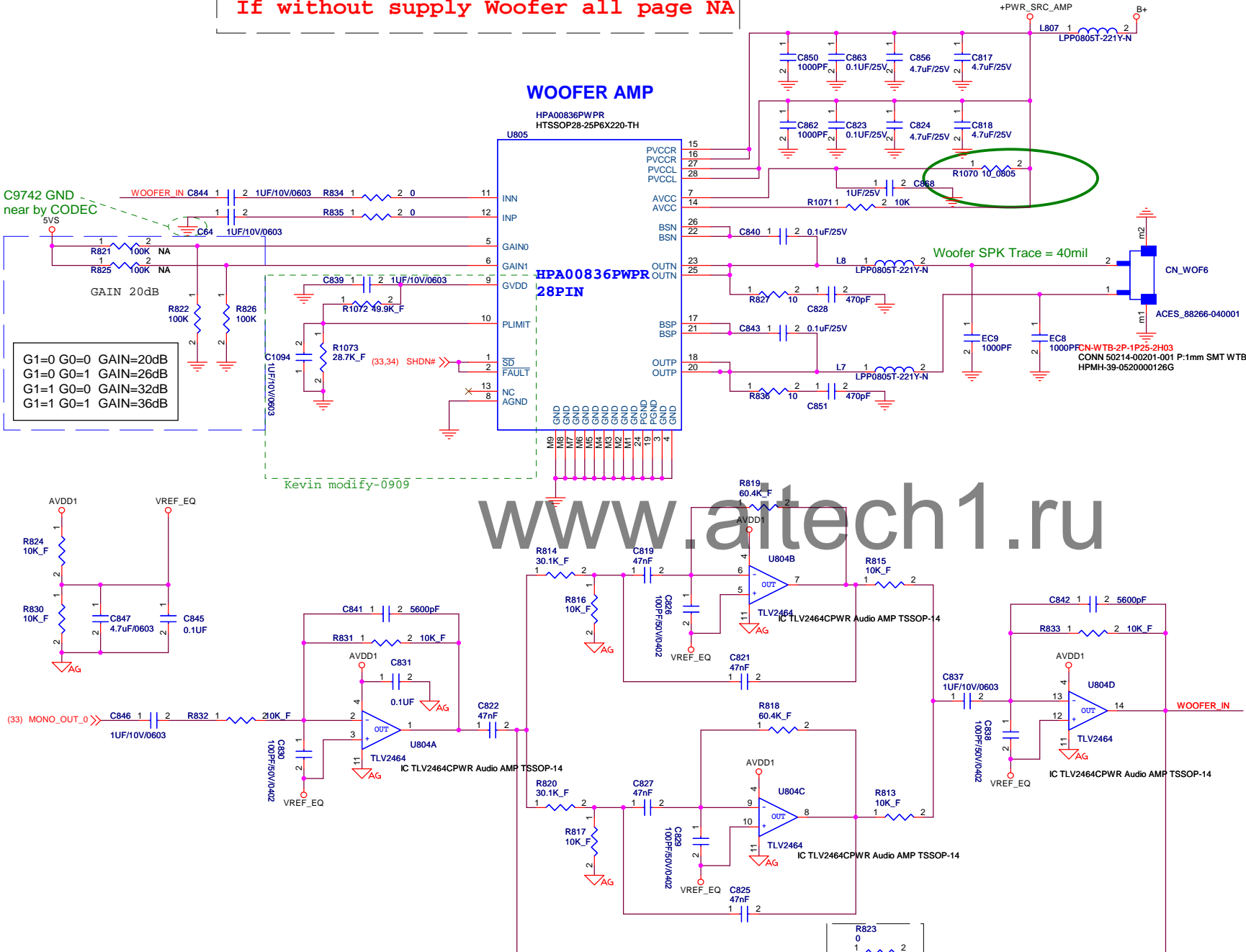
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Project Name : H710DI1		Title : RESERVE	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
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Audio CODEC



If without supply Woofer all page NA



NA
Always NA

FLEX Computing

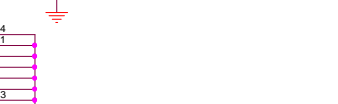
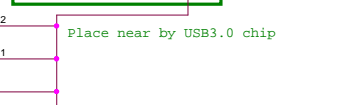
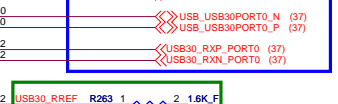
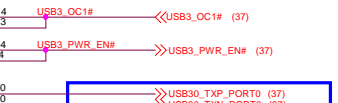
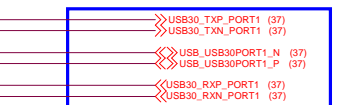
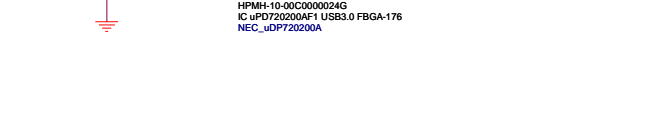
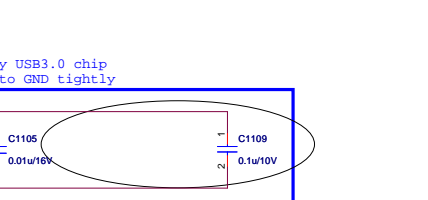
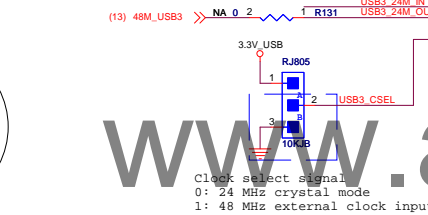
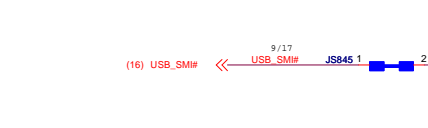
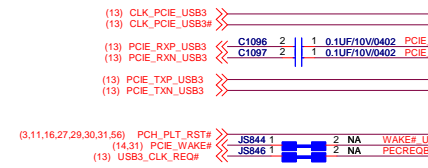
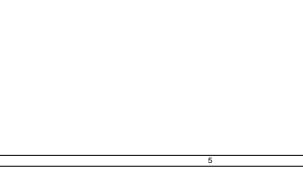
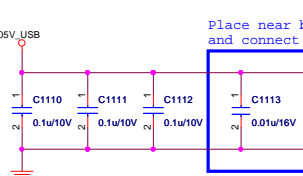
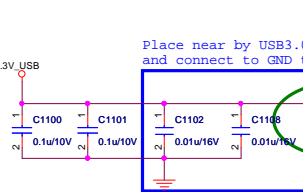
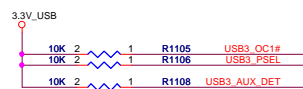
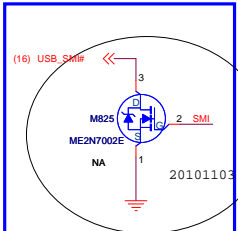
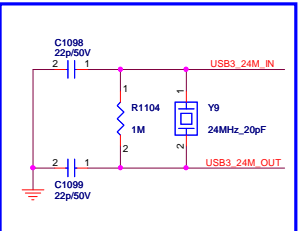
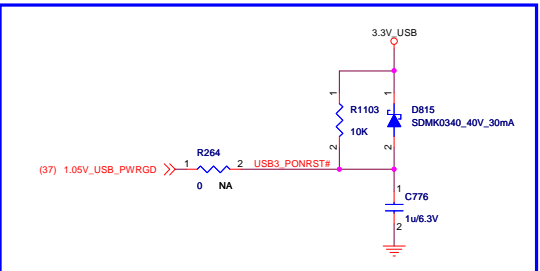
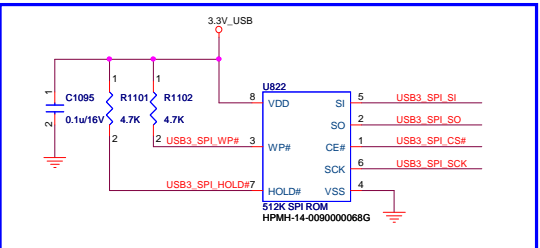
Project Name : H710DI1	Title : Audio 3/3 WOOFER AMP
---------------------------	---------------------------------

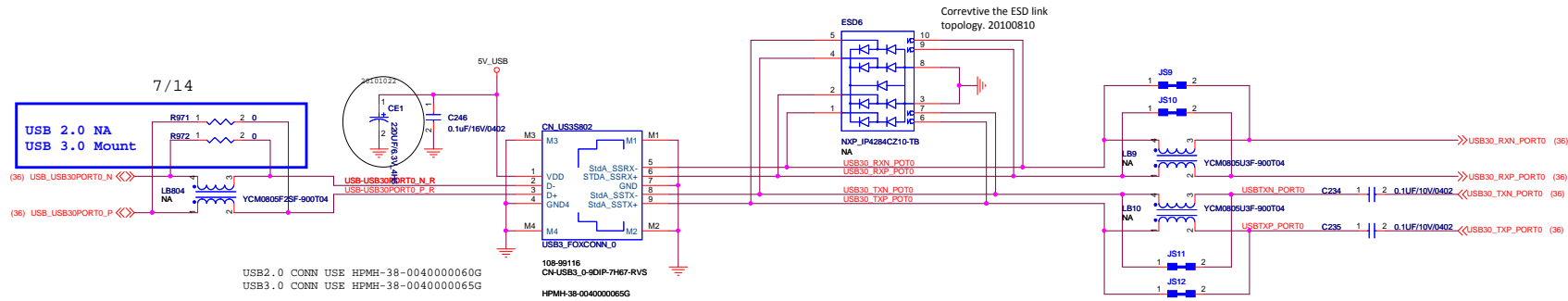
Size :	Document Number : HPMH-40GAB6600-B130
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Rev :	B
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Date: Monday, November 08, 2010 Sheet : 35 of 63

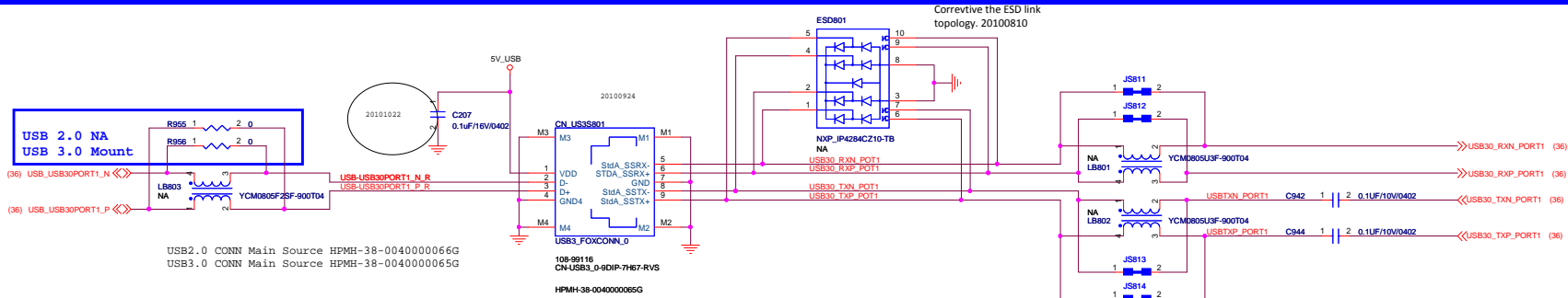
USB3.0 NEC uDP720200





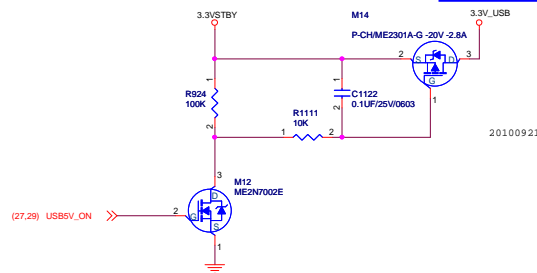
USB 2.0 2nd Source
HPMH-38-00400000078G
HPMH-38-00400000080G
HPMH-38-00400000087G

USB 3.0 2nd Source
HPMH-38-00400000068G
HPMH-38-00400000088G

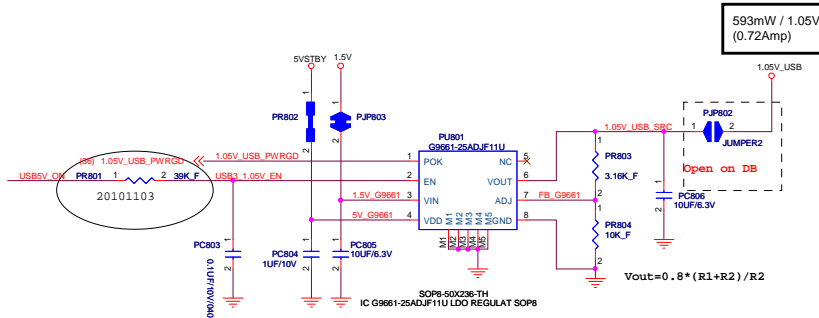


USB3.0 3.3V

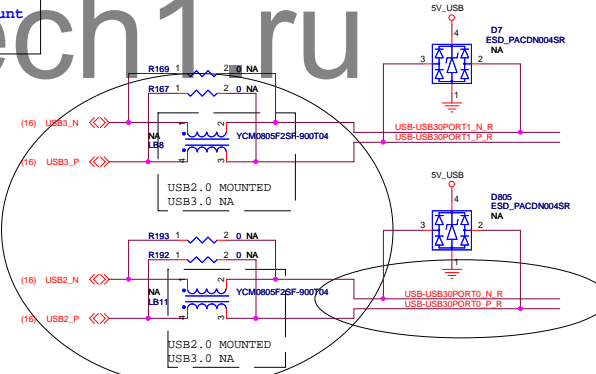
500mW / 3.3V
(0.151Amp)



USB3.0 1.05V_USB

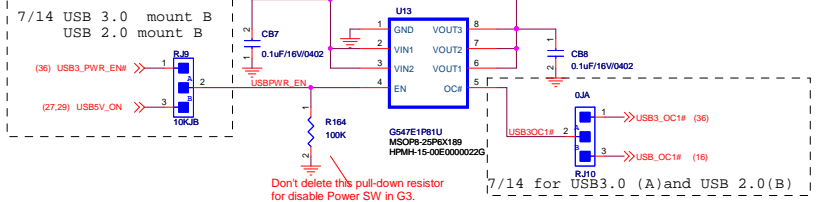


USB 2.0 Mount
USB 3.0 NA



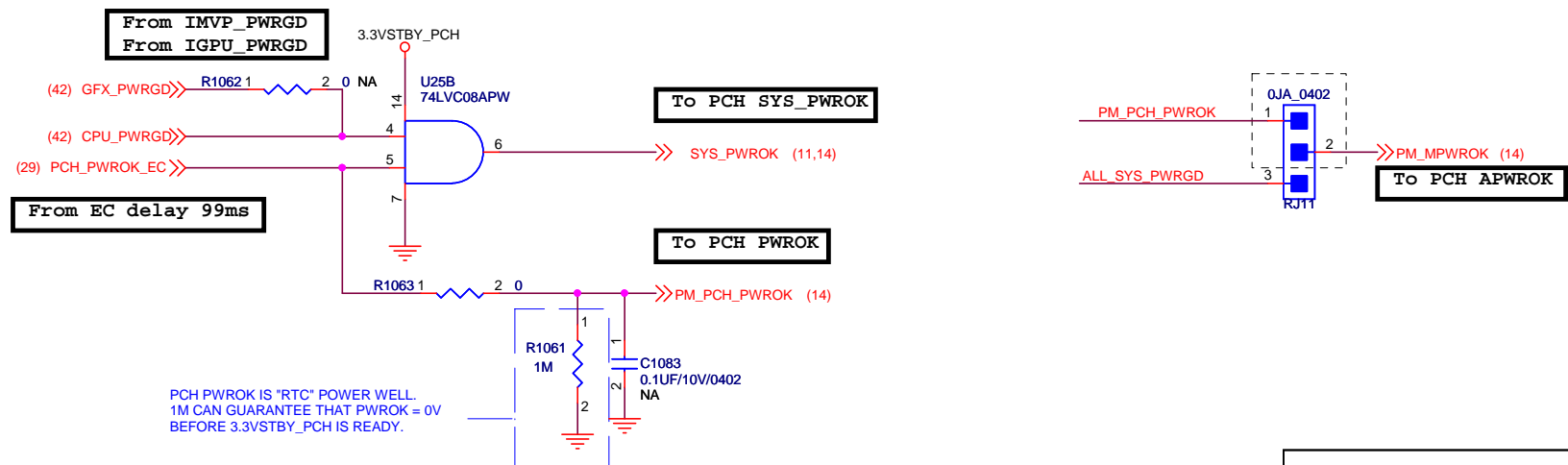
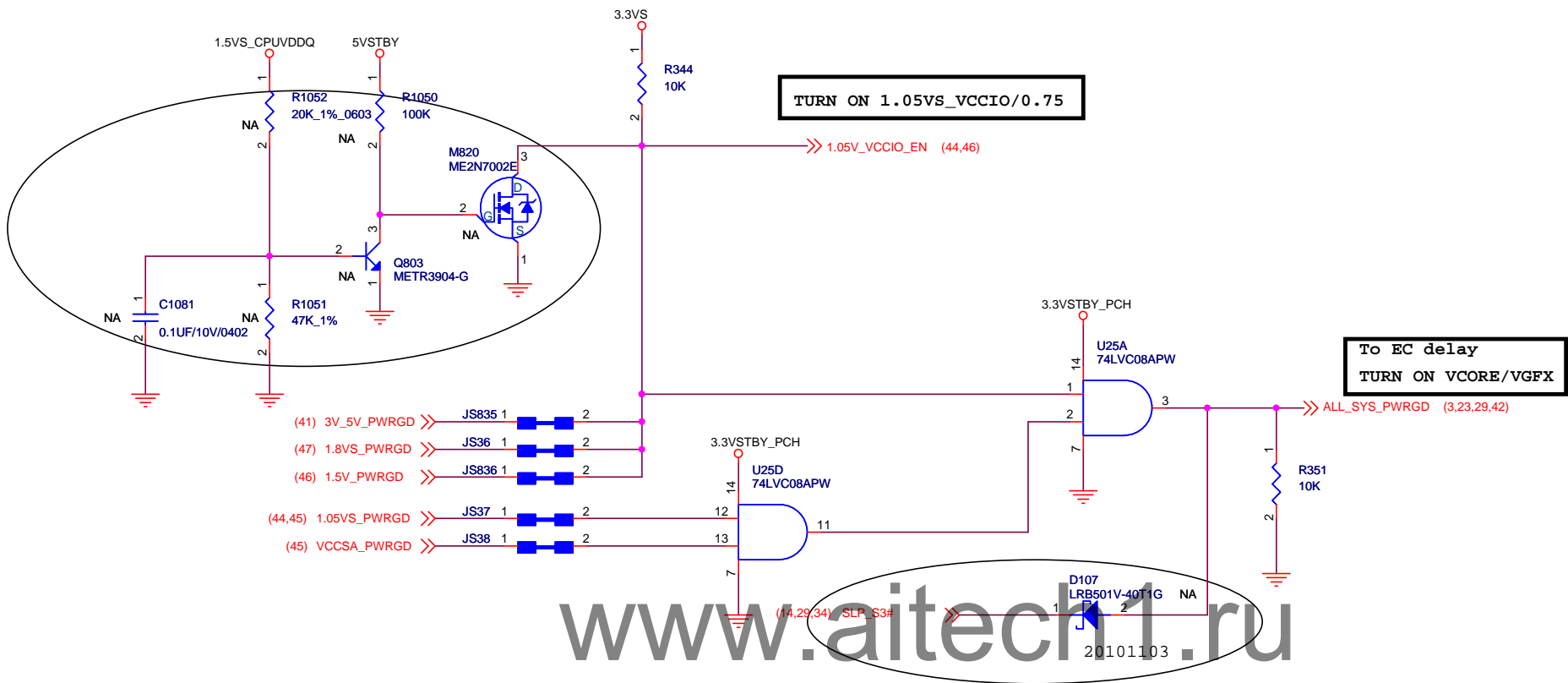
USB POWER SW

7/14 for USB3.0 and USB 2.0



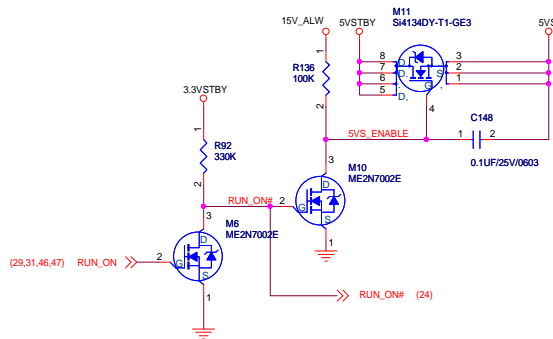
FLEX Computing

Project Name : H710D11
Title : USB30_CNN/PWR_SW/1.1V/3.3V
Size : Document Number : HPMH-40CAB6600-B130
Date : Monday, November 08, 2010
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Sheet : 37 of 63

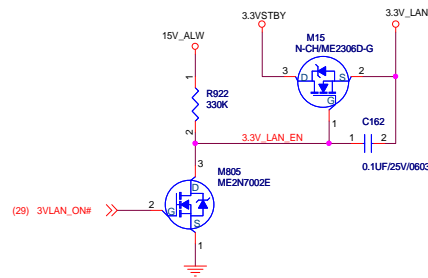


FLEXComputing

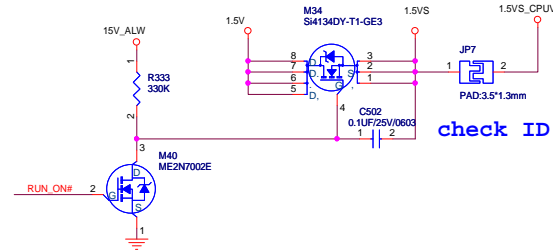
Project Name : H710D11		Title : POWER_GOOD	
Size : Custom	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 38	of 63



TDC: ?A



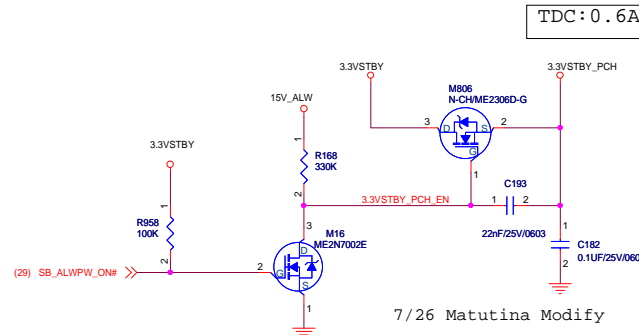
TDC: 0.3A



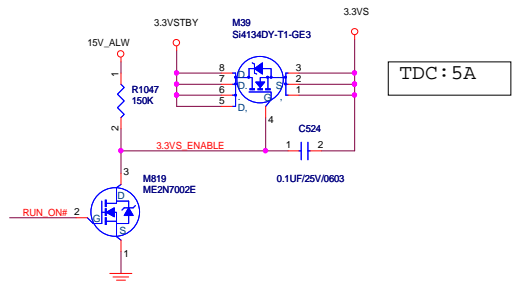
TDC: ?A

check ID

ME4626 :
Vgs(th): 3V(max)
Rds(on): 3.2m@Vgs = 10V (Max)
Rds(on): 4.9m@Vgs = 4.5V (Max)
Id : 23A

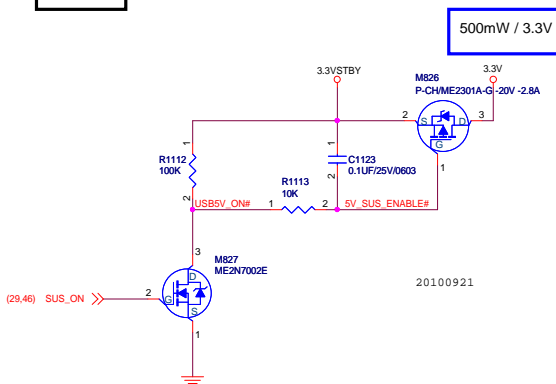


TDC: 0.6A



TDC: 5A

3.3V



500mW / 3.3V

ME2306D:

Vgs(th) : 1.0V(min),3.0V(max)
Rds(on) : 31m @ Vgs = 10V(MAX)
Rds(on) : 52m @ Vgs = 4.5V(MAX)
Id : 3.9A(Max)

ME4894-G:

Vgs(th) : 1.0V(min),3.0V(max)
Rds(on) : 11.7m @ Vgs = 10V (MAX)
Rds(on) : 18.2m @ Vgs = 4.5V(MAX)
Id : 11.5A(Max)

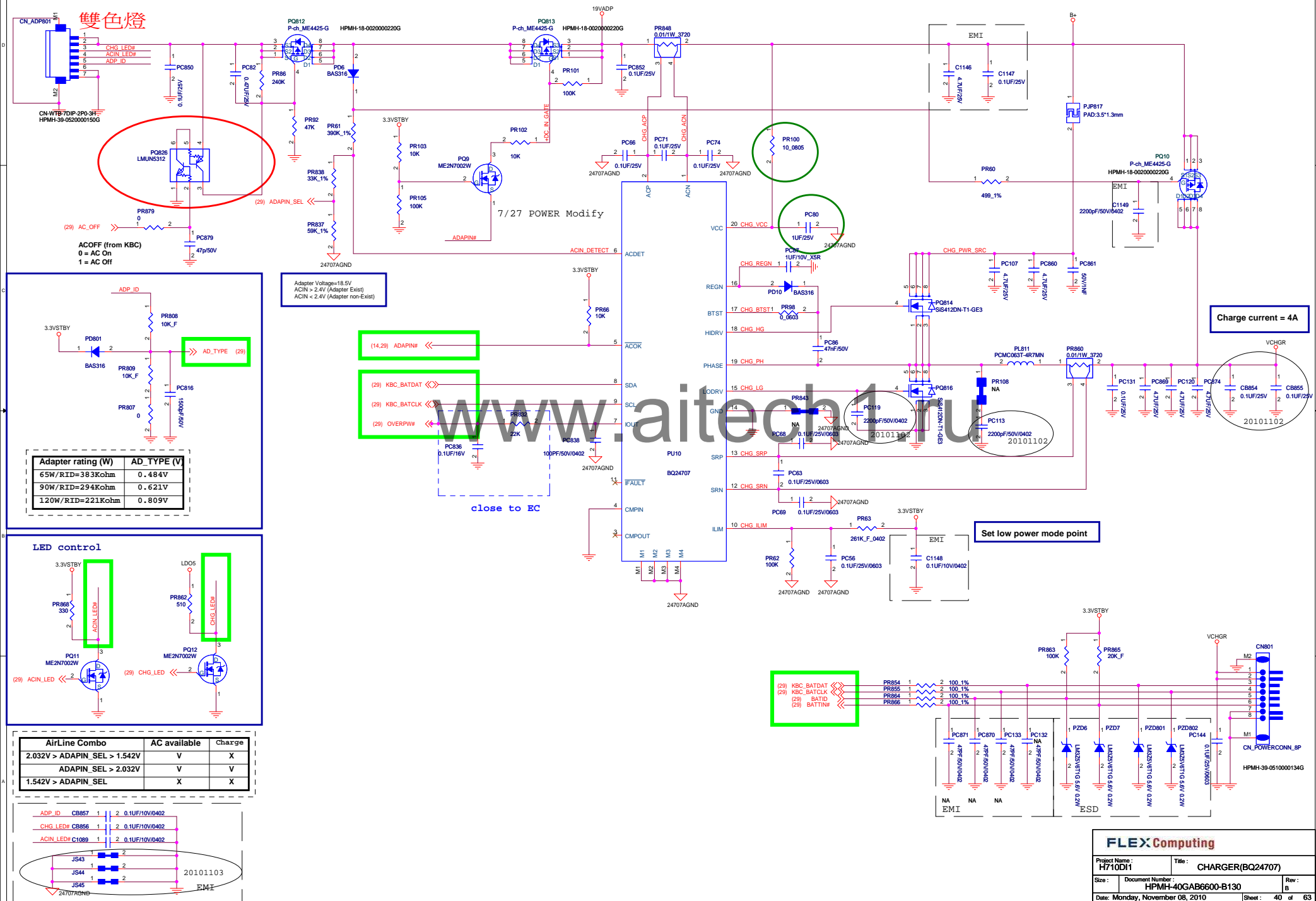
ME2301A:

Vgs(th) : -0.9V(max)
Rds(on) : 75m @ Vgs = -4.5V(MAX)
Id : -2.8A(Max)

7/26 Matutina Modify

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Charger



5V / 3.3VSTBY

Freq=300KHz
TDC = 7 A
OCP = 10 A

* Options 1.
5VSTBY

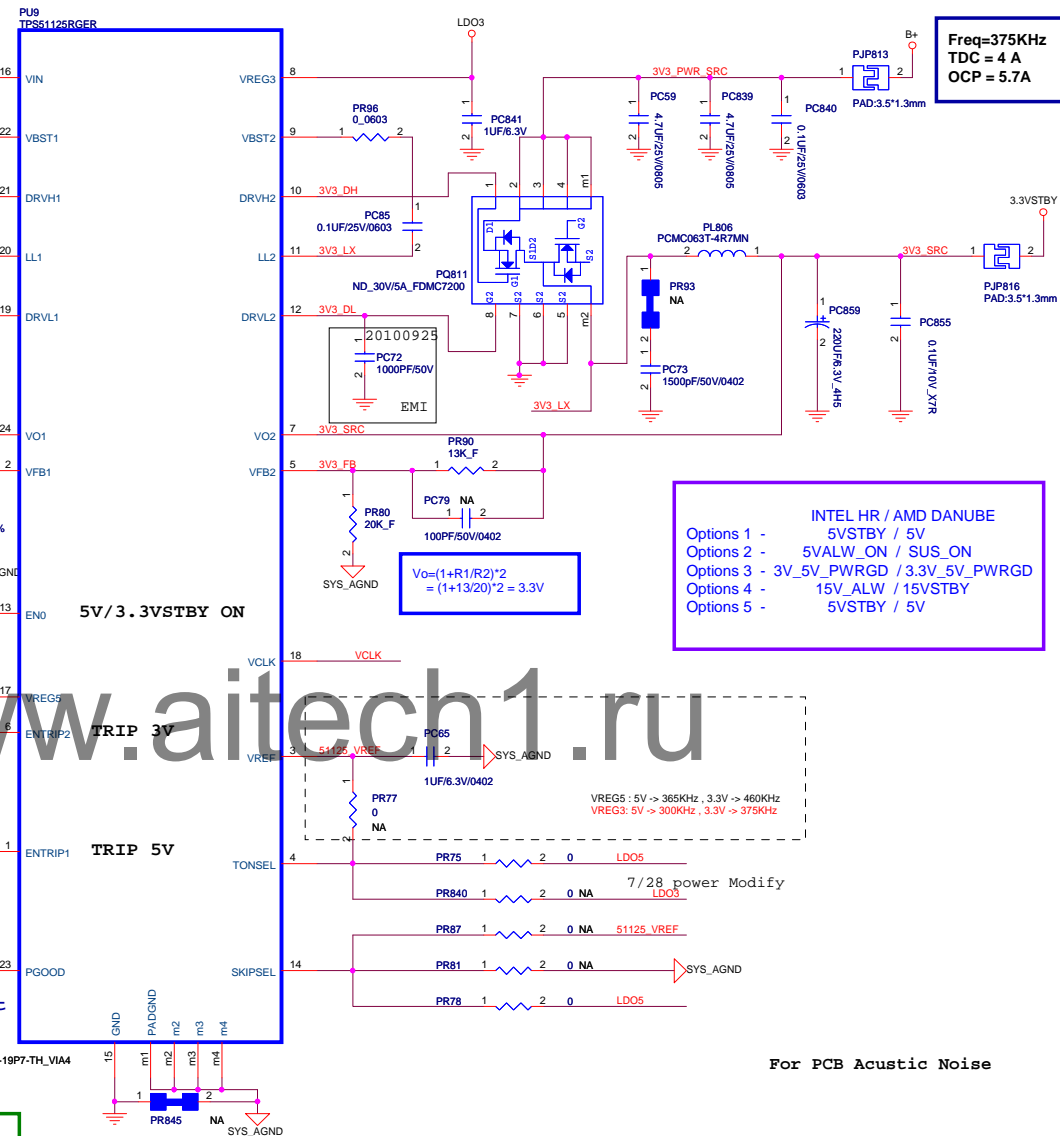
* Options 2.

* Options 3.

Table 3. Enabling State

EN0	ENTRIP1	ENTRIP2	VREF	VREG5	VREG3	CH1	CH2	VCLK
GND	Don't Care	Don't Care	Off	Off	Off	Off	Off	Off
R to GND	Off	Off	On	On	On	Off	Off	Off
R to GND	On	Off	On	On	On	On	Off	Off
R to GND	Off	On	On	On	On	Off	On	Off
R to GND	On	On	On	On	On	On	On	Off
Open	Off	Off	On	On	On	Off	Off	Off
Open	On	Off	On	On	On	On	Off	On
Open	Off	On	On	On	On	Off	On	Off
Open	On	On	On	On	On	On	On	On

PU3-m1
For layout request, no connect anything.

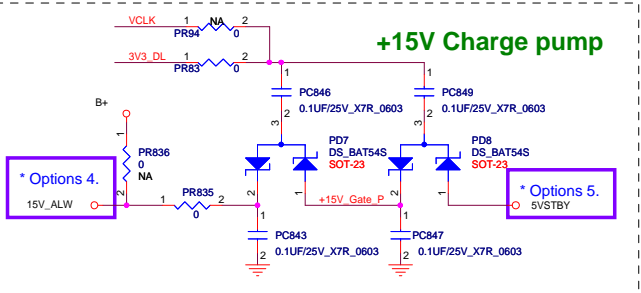


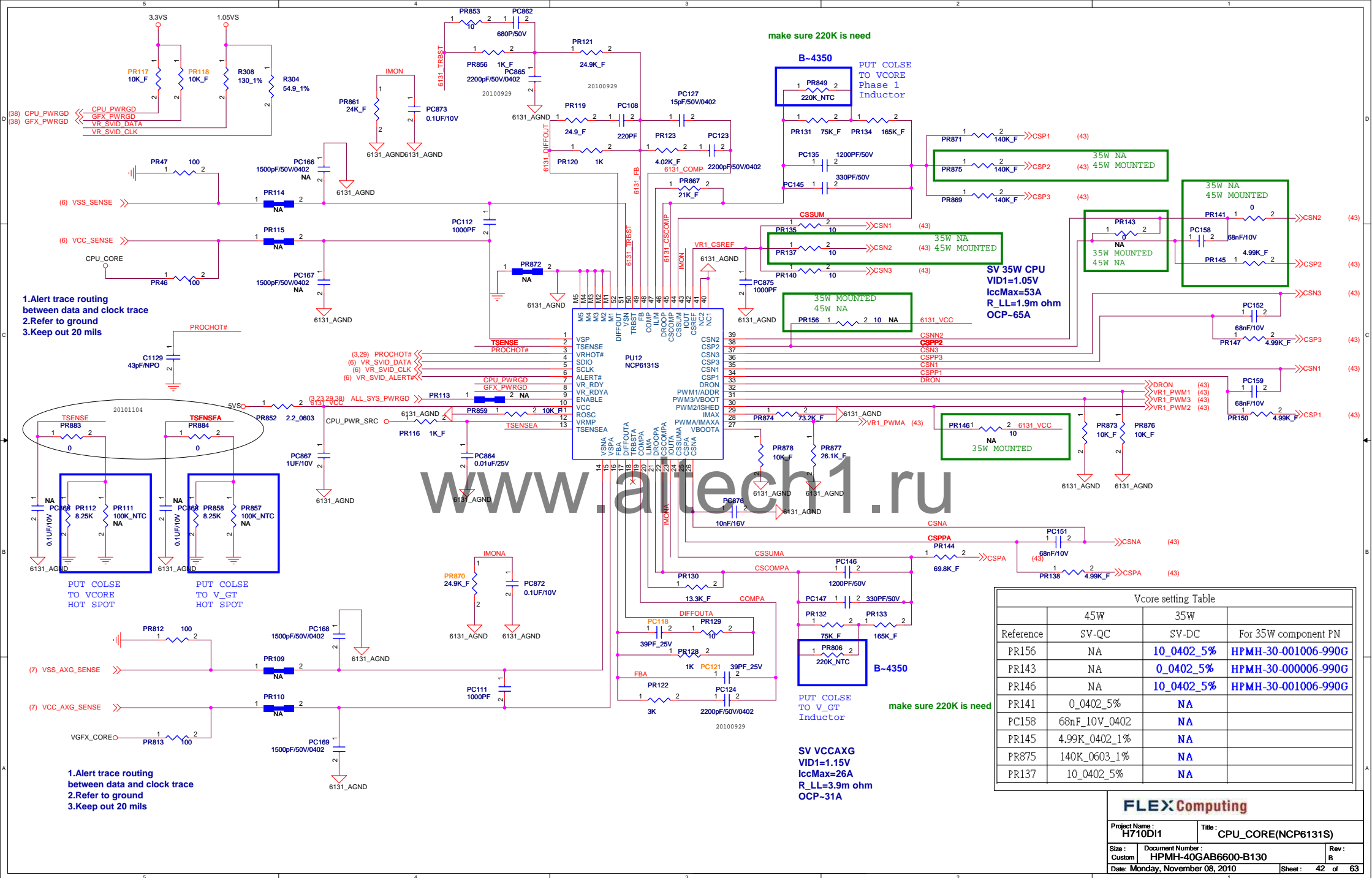
Freq=375KHz
TDC = 4 A
OCP = 5.7 A

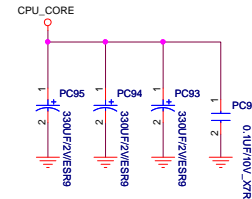
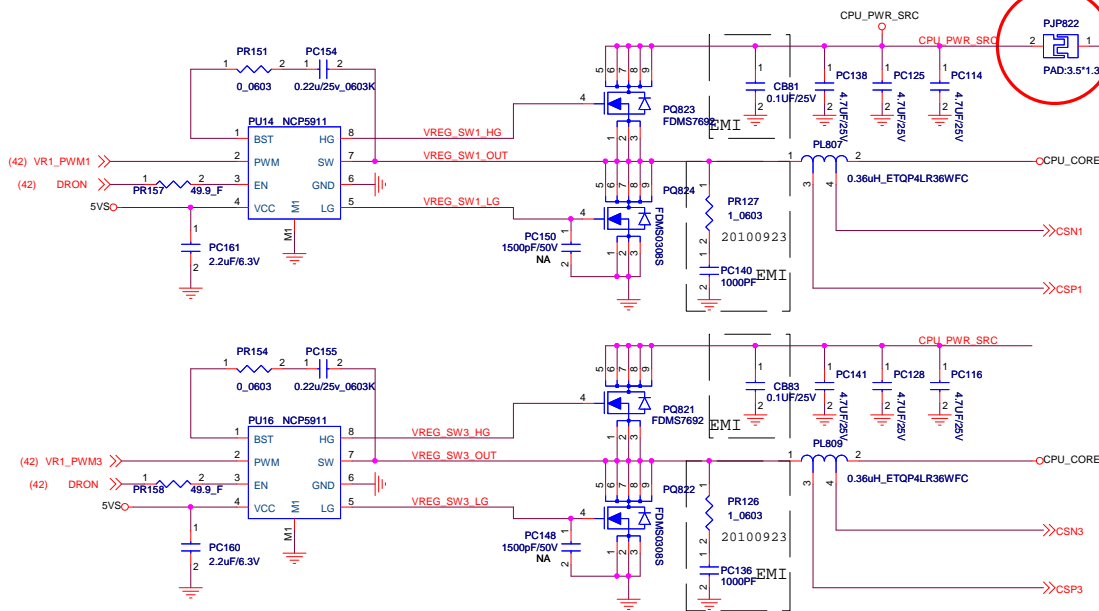
INTEL HR / AMD DANUBE
Options 1 - 5VSTBY / 5V
Options 2 - 5VALW_ON / SUS_ON
Options 3 - 3V_5V_PWRGD / 3.3V_5V_PWRGD
Options 4 - 15V_ALW / 15VSTBY
Options 5 - 5VSTBY / 5V

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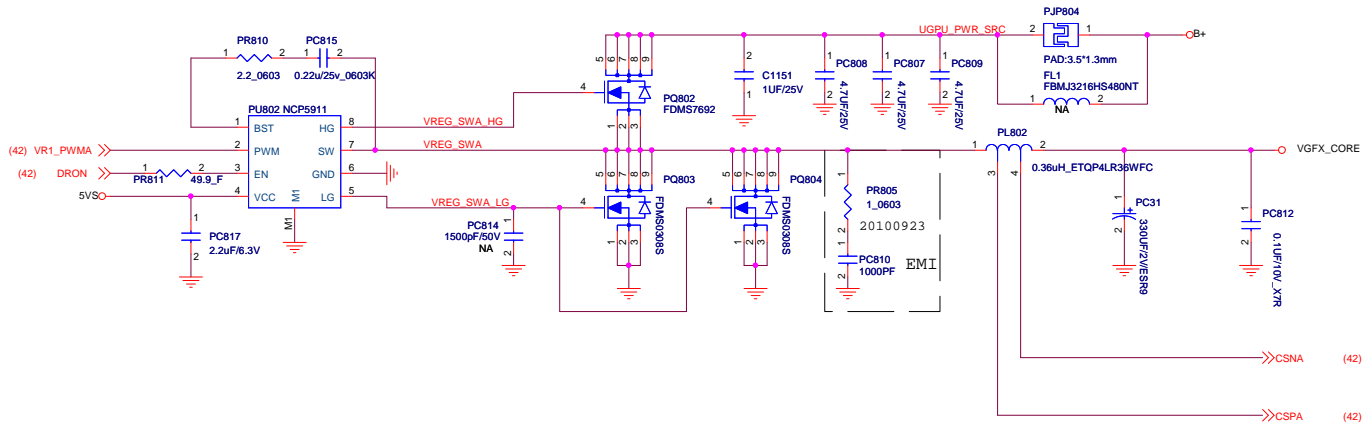
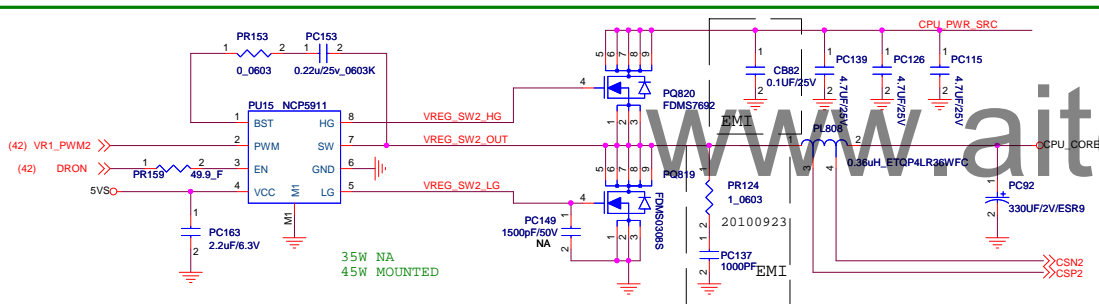
For PCB Acoustic Noise







Vcore setting Table			
	45W	35W	
Reference	SV-QC	SV-DC	For 35W component PN
PU15	NCP5911	NA	
PR153	0_0603_5%	NA	
PC153	0.22UF_25V_0603	NA	
PR159	49.9_0402_1%	NA	
PC163	2.2UF_6.3V_0603	NA	
PQ820	FDMS7692	NA	
PQ819	FDMS0308S	NA	
PL808	0.36uH	NA	
PR874	73.2K_0402_1%	41.2K_0402_1%	HPMH-30-141221-990G
PR861	24K_0402_1%	24.9K_0402_1%	HPMH-30-124921-990G
PR867	21K_0402_1%	12.4K_0402_1%	HPMH-30-112421-990G



1.05VS_VCCIO
1.05VS

(38,45) 1.05VS_PWRGD

(38,46) 1.05V_VCCIO_EN

$$I_{OCP} = ((PR4551 * 10) / 8 * R_{ds(on)}) + I_{O(max)} / 6 = 18.4A$$

Freq=430KHz

RF pull down to GND with resistor : Auto-skip
RF connect to PGOOD with resistor : Force CCM

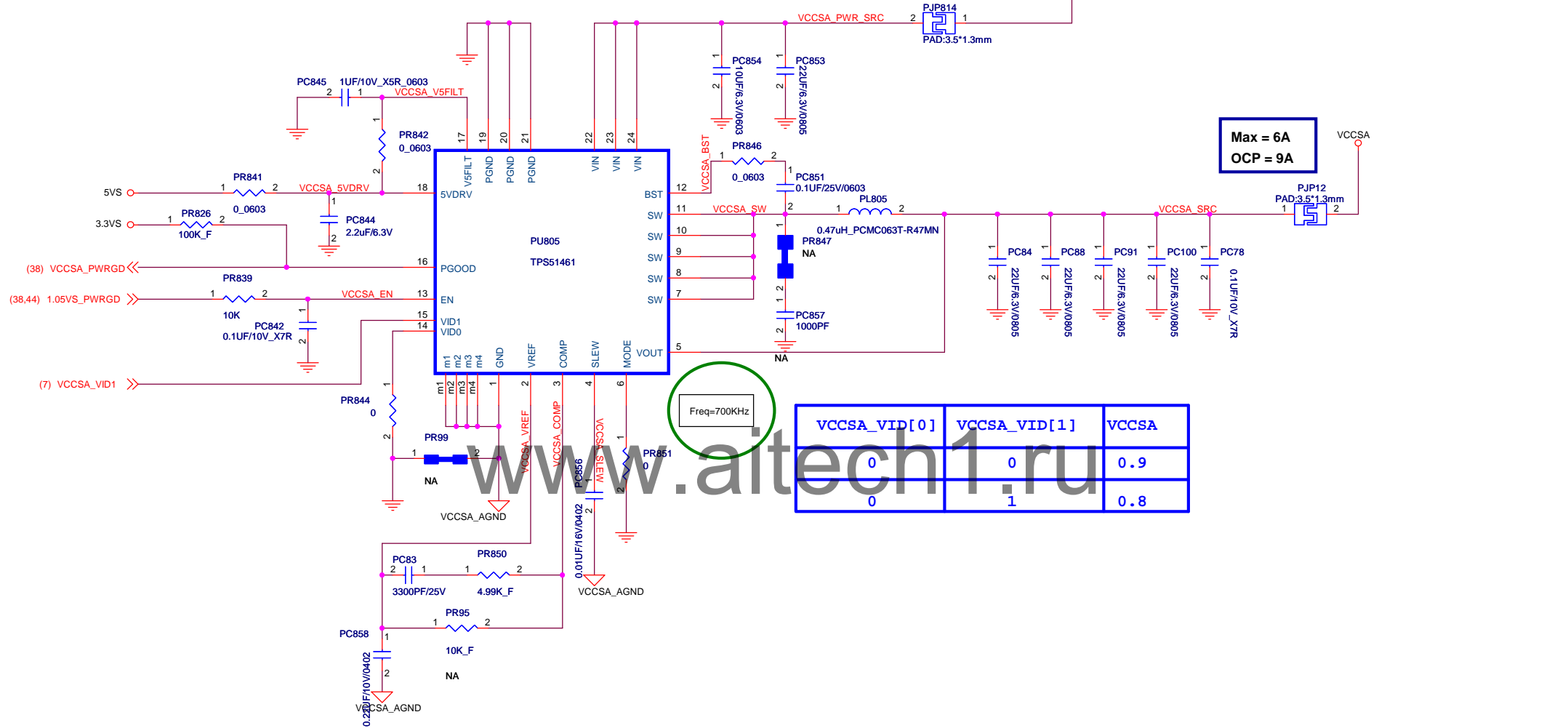
$$V_o = 0.75 * (1 + (PR529 / PR531)) = 0.75 * (1 + 0.47) = 1.107V$$

TDC=12.87A
OCP=15.54A

FLEX Computing

Project Name : H710DI1		Title : 1.05VS(TPS51218)	
Size : Custom	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet: 44 of 63	

VCCSA



1.5V

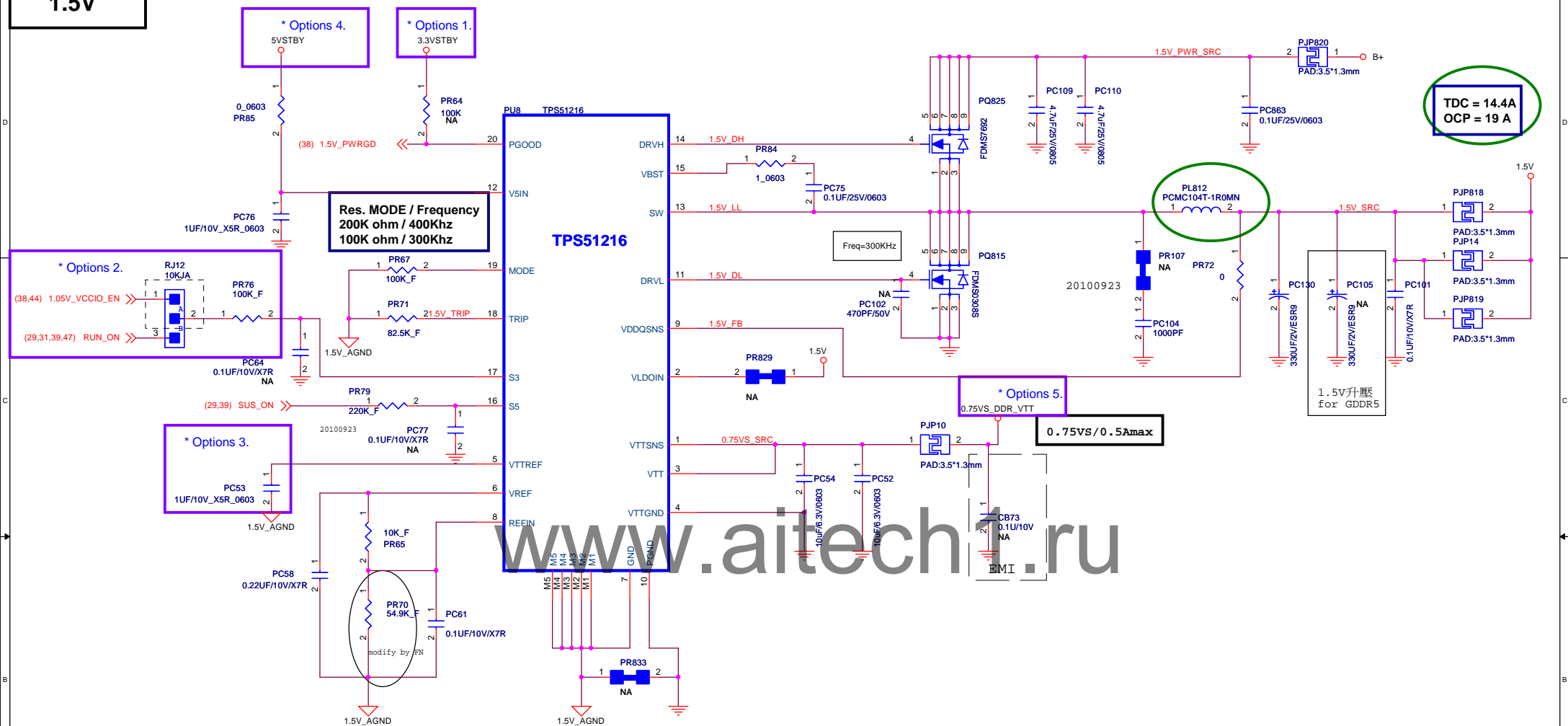


Table 1. S3 and S5 Control Table

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0 (high-Z)
S4/S5	L	L	0 (discharge)	0 (discharge)

INTEL HR / AMD DANUBE

Options 1 - 3.3VSTBY / 3.3V

Options 2 - RUN_ON / SUS_ON

Options 3 - DDR_VTTR / V_DDR_VTT

Options 4 - 5VSTBY / 5V

Options 5 - 0.75VS_DDR_VTT / 0.75V_DDR_VTT

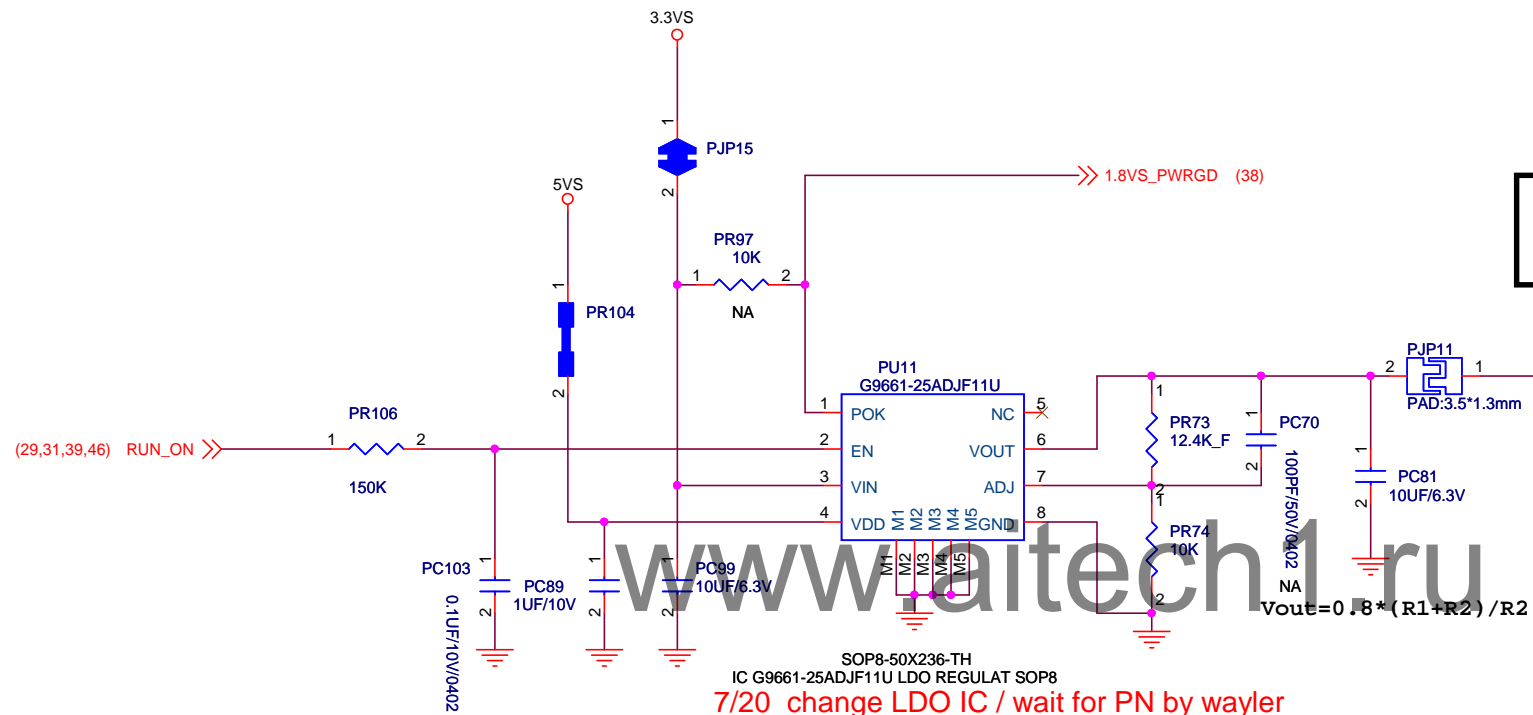
FLEX Computing

Project Name :
H710D11Title :
DDR_PWR(TPS51216)Size :
Document Number :
HPMH-40GAB6600-B130Rev :
B

Date: Monday, November 08, 2010

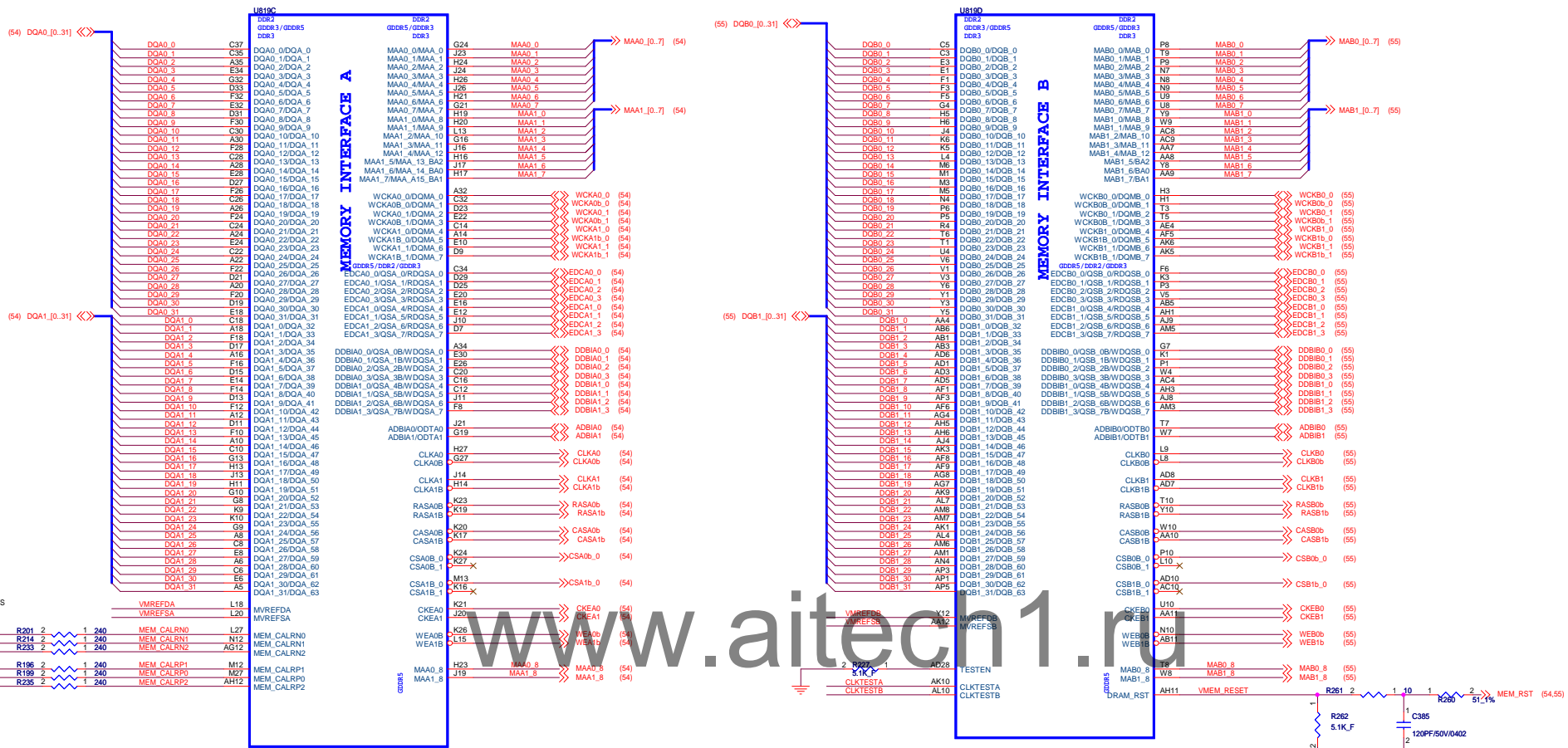
Sheet: 46 of 63

1.8VS



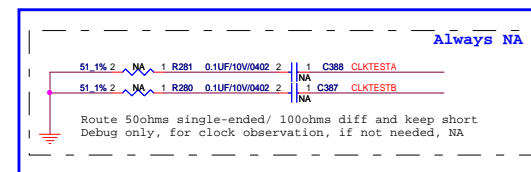
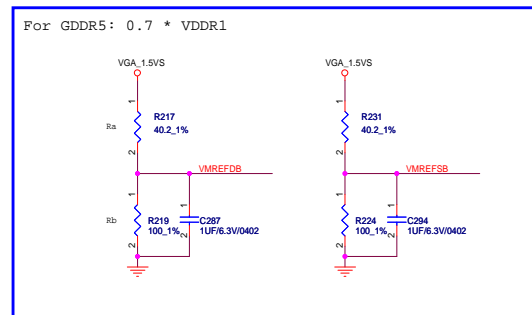
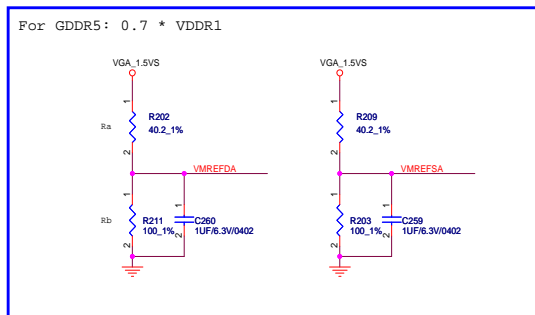
FLEX Computing

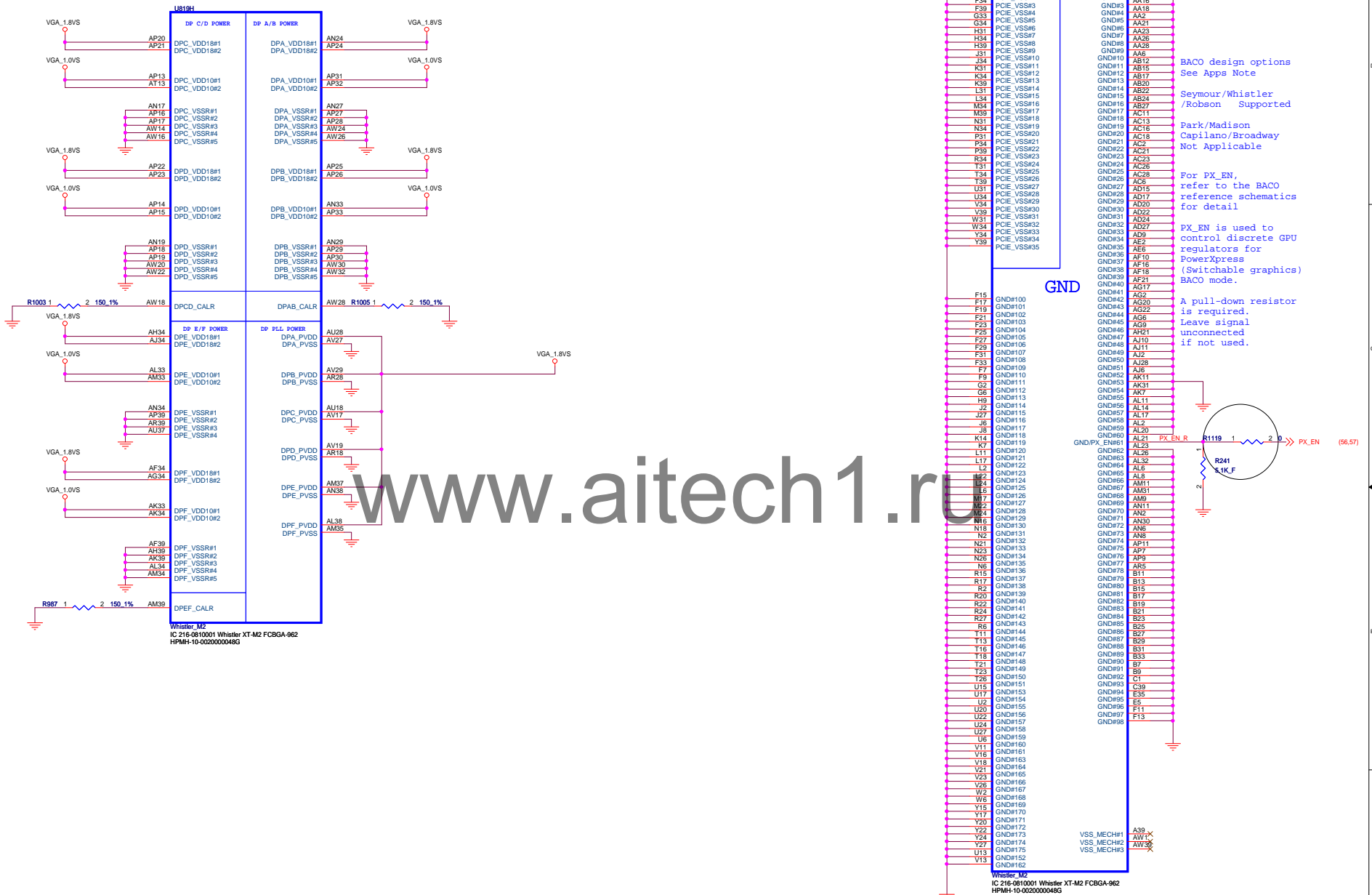
Project Name : H710DI1		Title : 1.8VS	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 47 of 63	



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

VRAM TYPE		PN
Hynix H5GQ1H24AFR-T2C	64MX16(32MX32)	HPMH-14-0030000001G
Hynix H5GQ2H24MFR-T2C	128MX16(64MX32)	HPMH-14-0030000002G
SAMSUNG K4G10325FE-HC04	64MX16(32MX32)	HPMH-14-0030000003G
SAMSUNG K4G20325FC-HC04	128MX16(64MX32)	HPMH-14-0030000004G
Elpida EDW1032BABG-50-F	64MX16(32MX32)	HPMH-14-0030000005G
Elpida EDW2032BABG-50-F	128MX16(64MX32)	HPMH-14-0030000006G

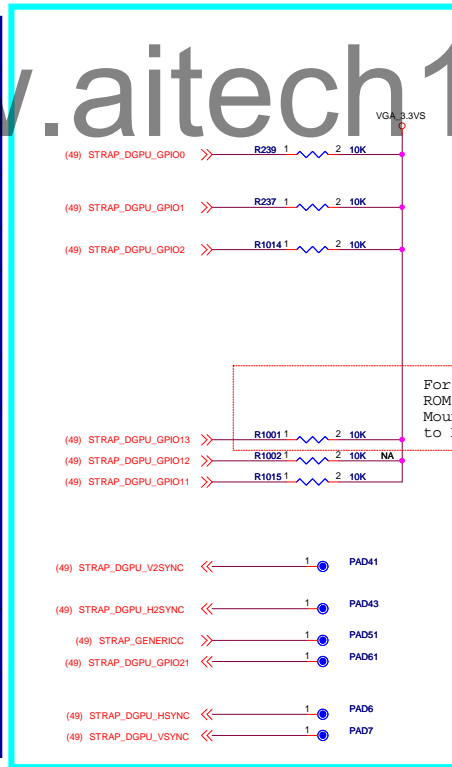


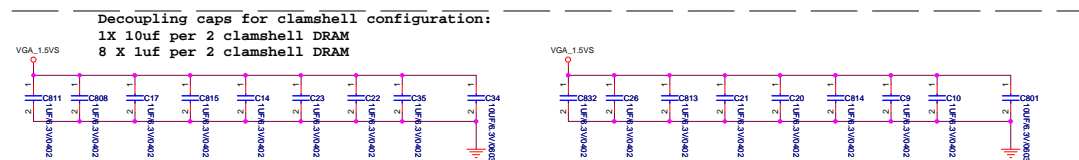
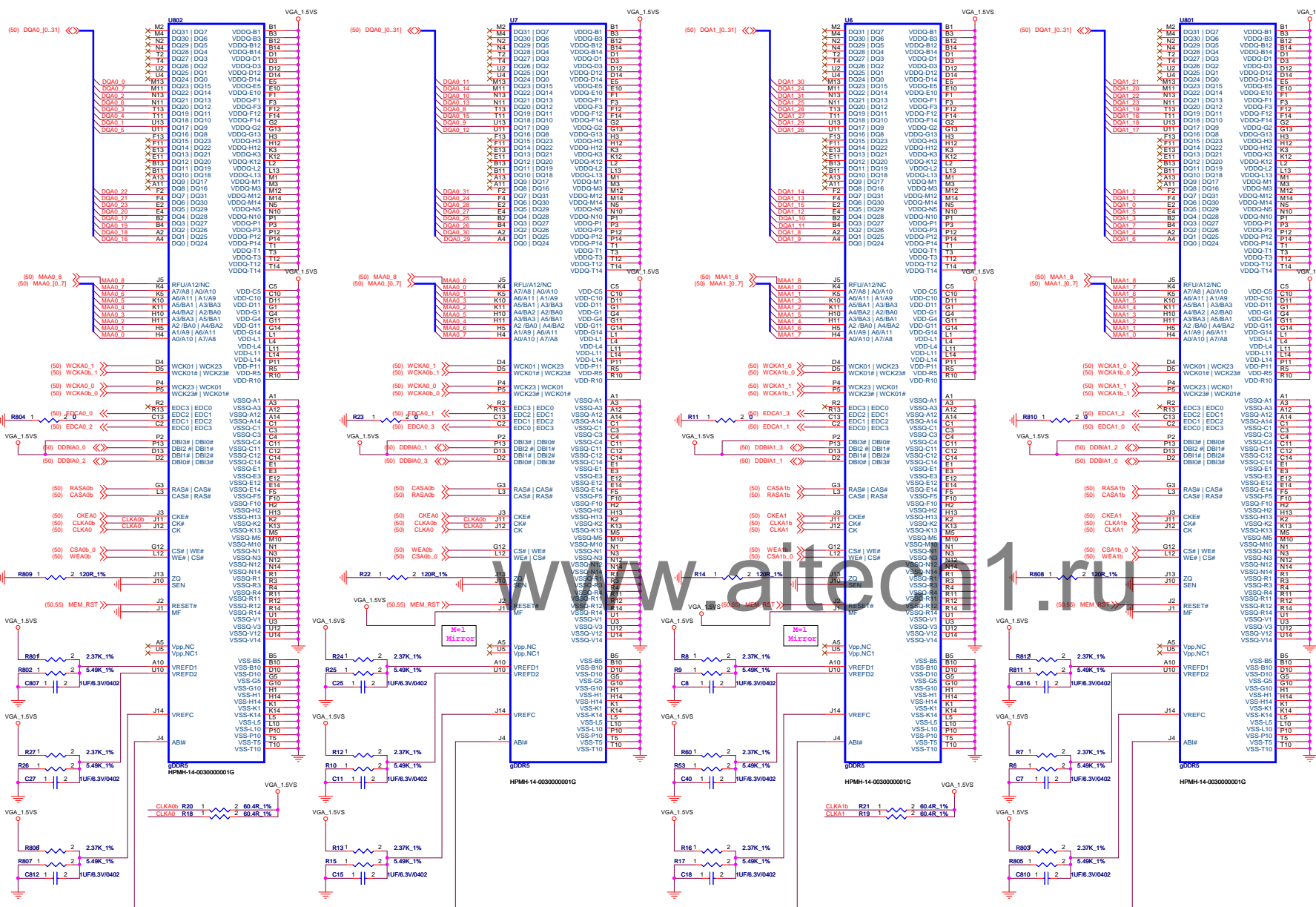


Signal	Seymour/Whistler	Robson/Park Medison/Capilano Broadway
Ball AC32 on M2	NC	DAC2 Output-C on M2 package
Ball AA29 on M2	NC	R2SET on M2 package
Ball AD32 on M2	NC	DAC2 Output- Y
Ball AG33 on M2	NC	A2VDD
Ball AD33 on M2	NC	A2VDDQ
Ball AF33 on M2	TSVSSQ	A2VSSQ
Ball AG33 AG32 on M2	NC	VDD2DI/VSS2DI
H2SYNC	GENLK_CLK: (3.3V) Reference clock input (3.3V) for pixel PLL received from frame-lock/ gen-lock interface	H2SYNC
V2SYNC	GENLK_VSYNC (3.3V) Frame timing indicator.Output to frame-lock/genlock interface	V2SYNC

Signal	Seymour/Whistler	Robson/Park Medison/Capilano Broadway
Ball AJ21 on M2 Ball AG13 on S3	SWAPLOCKA SwaplockA/B signals can be optionally used on a multi-GPU design with multiple display outputs to allow all displays in a group (group A or group B) to update at the same time and have synchronous left/right stereo timing. Genlock of the GPUs is also needed, either via a genlock system, or by feeding all GPUs with the same reference clock. Also connecting SwaplockB is preferred but not required. SwaplockA/B are open drain, 3.3V signals. If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AJ21 is NC on M2 packages Ball AG13 is R2SET on S3 package
Ball AK21 on M2 Ball H12 on S3	SWAPLOCKB - see above On a multi-gpu design, SwaplockB from all GPUs are connected together with an external pull-up resistor (10K Ohms). If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AK21 is NC on M2 packages Ball AH12 is DAC2 Output- on S3 package

CONFIGURATION STRAPS				
STRAPS	PIN	DESCRIPTION	ASIC Deault	Status
TX_PWRS_ENB	GPIO0	Transmitter (Tx) power savings enable. 0: 50% Tx output swing 1: Full Tx output swing (DEFAULT)	0 Internal Pull Down	Mounted
TX_DEEMPH_EN	GPIO1	PCI Express transmitter deemphasis enable. 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (DEFAULT)		Mounted
RESERVED	GPIO2	0: PCIe device as 2.5 GT/s capable 1: PCIe device as 5.0 GT/s capable (DEFAULT)		Mounted
VGA_DIS	GPIO9	VGA disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space): 0: VGA Controller capacity enabled (DEFAULT) 1: The device will not be recognized as the system's VGA controller		NA NA
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable the external BIOS ROM device: 0 - Disable external BIOS ROM device (DEFAULT) 1 - Enable external BIOS ROM device		Mounted
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	BIOS_ROM_EN = 1, Config[2:0] defines the ROM type. BIOS_ROM_EN = 0, Config[2:0] defines the primary memory aperture size Size of the primary memory apertures CONFIG[2:0] 128 MB 000 256 MB 001 (DEFAULT) 64 MB 010 32 MB 011		Mounted NA Mounted
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS L: Ignore VIP Device Strap (DEFAULT) H: Enable VIP Device Strap		NA
RESERVED RESERVED RESERVED RESERVED	H2SYNC GENERICC GPIO8 GPIO21_BB_EN			NA NA NA NA
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function (DEFAULT) 0 1 Audio for DisplayPort only 1 0 Audio for DisplayPort and HDMI if dongle is detected 1 1 Audio for both DisplayPort and HDMI		NA NA

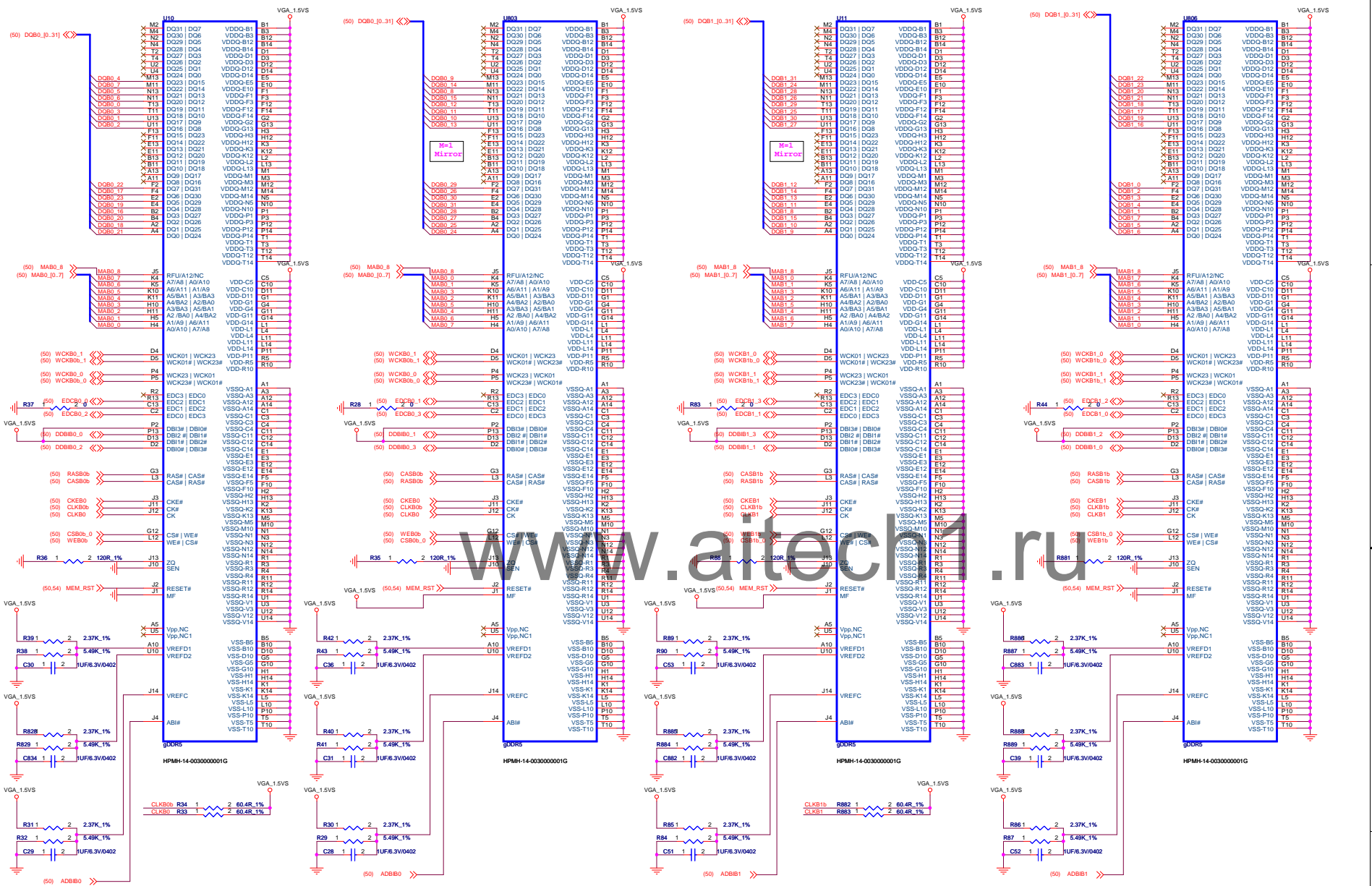




NA for Seymour

DDR5 Memory Channel A X16 Mode

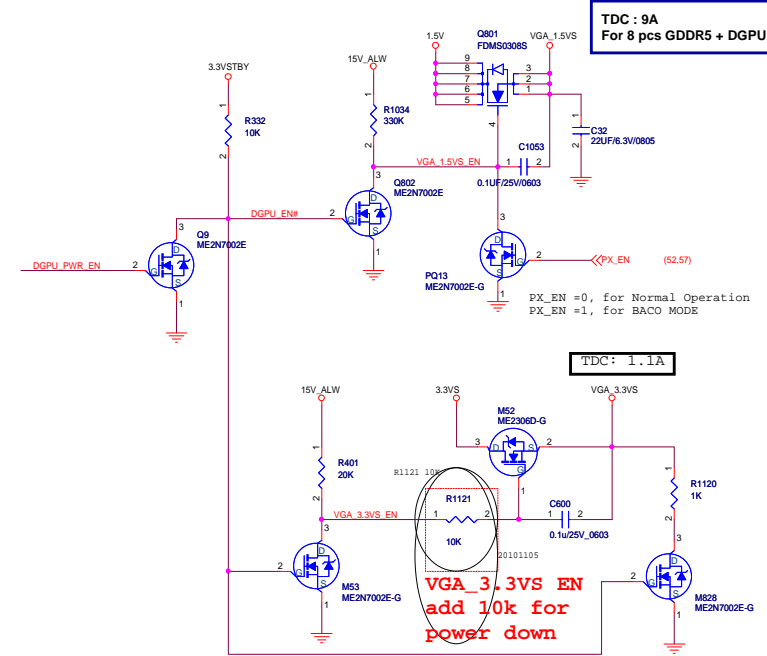
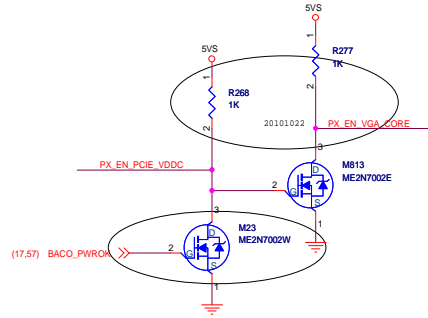
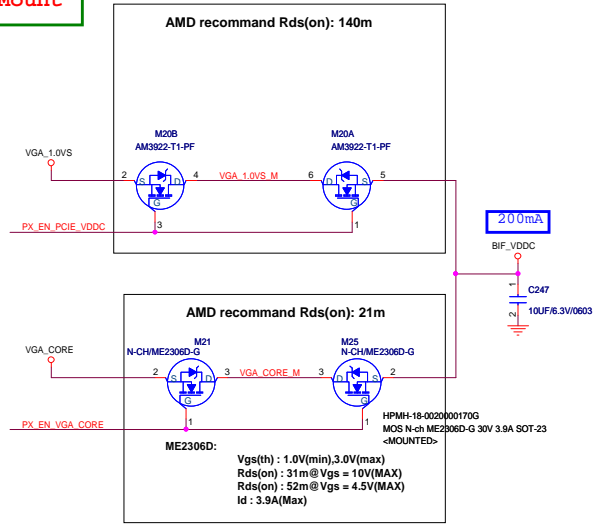
FLEX Computing	
Project Name:	H710D1
Title:	Capitan_VRAM GDDR5 64MX16 A
Size:	Document Number:
Date:	Monday, November 08, 2010
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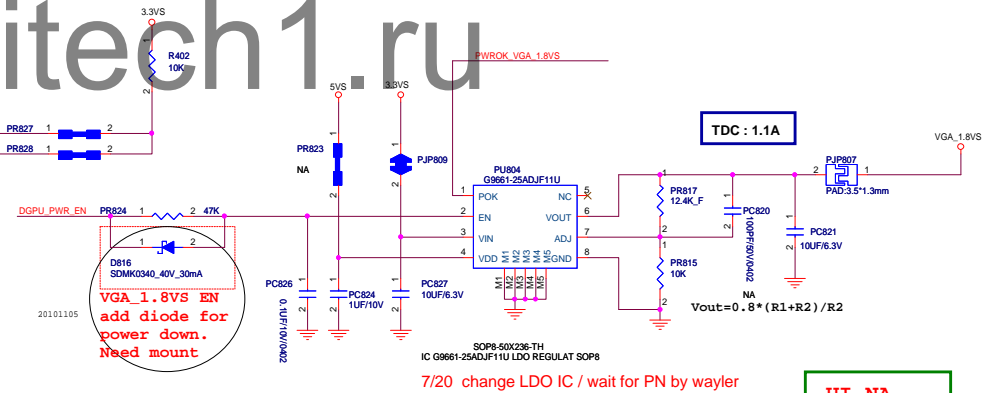
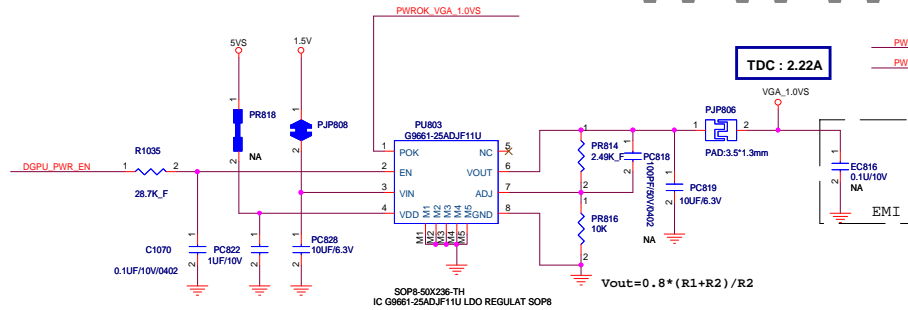
GDDR5 Memory Channel B X16 Mode

Decoupling caps for clamshell configuration:
 1X 10uf per 2 clamshell DRAM
 8 X 1uf per 2 clamshell DRAM

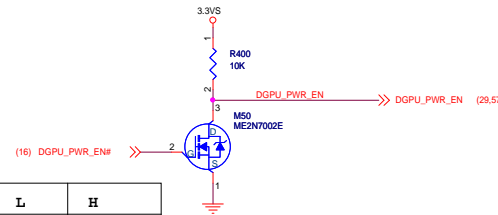
UI NA
DI Mount



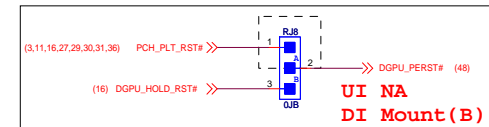
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UI NA
DI Mount



L	H
DGPU ON	DGPU OFF



VID4 (PP2) (GPIO16)	VID3 (PP1) (GPIO20)	VID2 (PP0) (GPIO15)	VGA_CORE
0	0	1	1.05V
1	0	0	0.900V

VID						V _{DAC} (V)
6	5	4	3	2	1	0
0	1	0	0	1	0	1.0500
0	1	1	0	0	0	0.9000

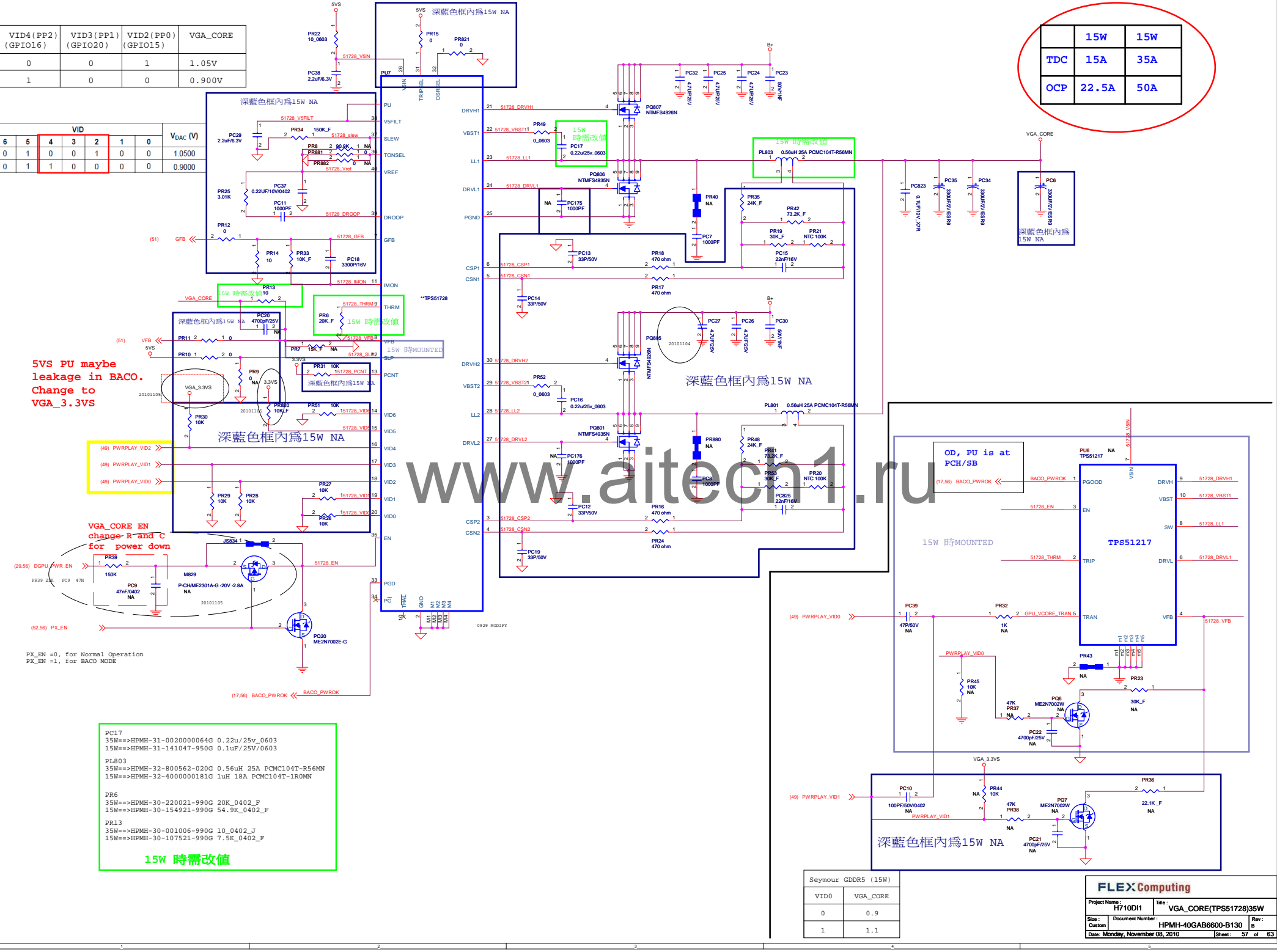
5VS PU maybe leakage in BACO. Change to VGA_3.3VS

VGA_CORE EN change R and C for power down

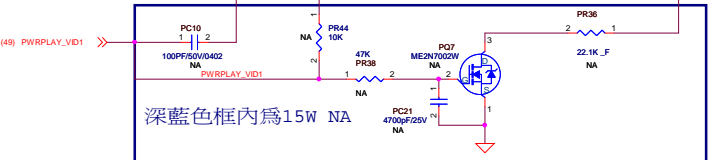
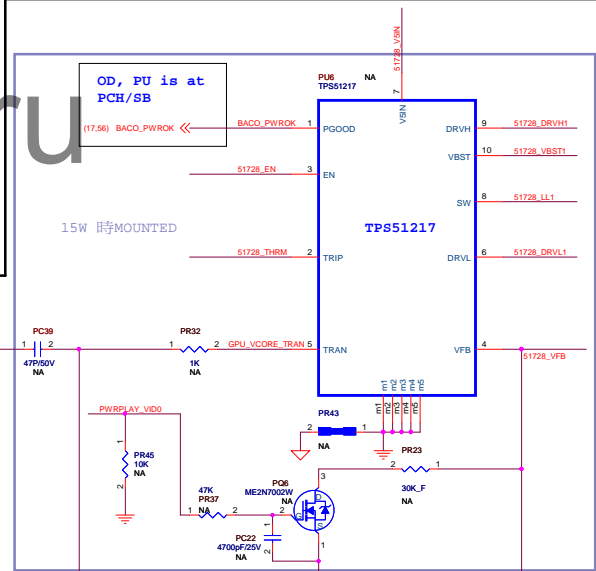
PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

PC17
35W==>HPMH-31-0020000064G 0.22u/25v_0603
15W==>HPMH-31-141047-950G 0.1uF/25V/0603
PL803
35W==>HPMH-32-800562-020G 0.56uH 25A PCMC104T-R56MN
15W==>HPMH-32-4000000181G 1uH 18A PCMC104T-1R0MN
PR6
35W==>HPMH-30-220021-990G 20K_0402_F
15W==>HPMH-30-154921-990G 54.9K_0402_F
PR13
35W==>HPMH-30-001006-990G 10_0402_J
15W==>HPMH-30-107521-990G 7.5K_0402_F

15W 時需改值

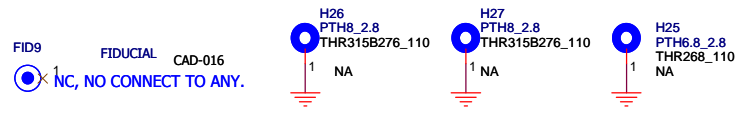


	15W	15W
TDC	15A	35A
OCF	22.5A	50A



Seymour GDDR5 (15W)	
VID0	VGA_CORE
0	0.9
1	1.1

FLEX Computing	
Project Name: H710D11	Title: VGA_CORE(TPS51728)35W
Size: Custom	Document Number: HPMH-40GAB6600-B130
Date: Monday, November 08, 2010	Rev: 8
Sheet: 57	of 63



FID802 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID11 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

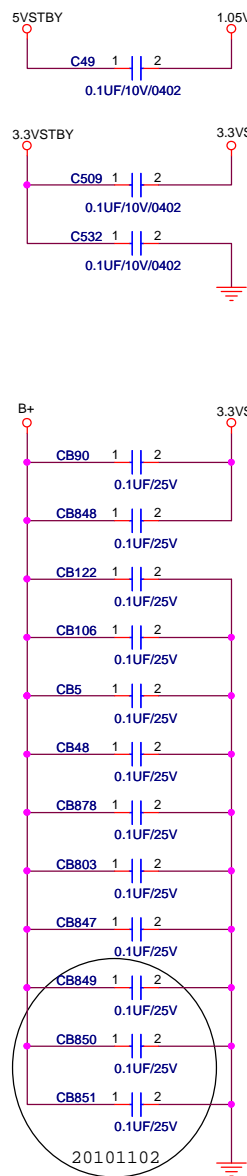
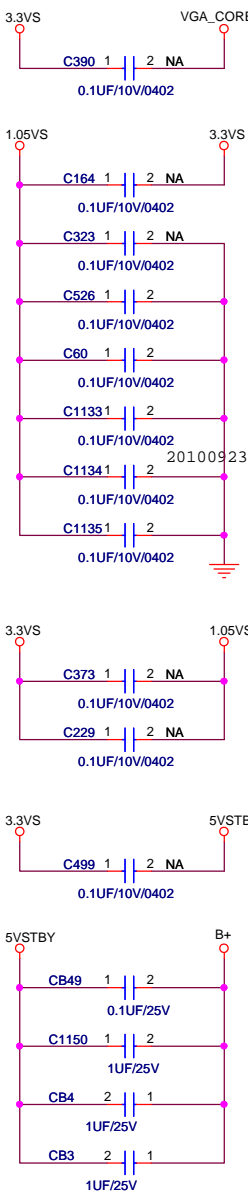
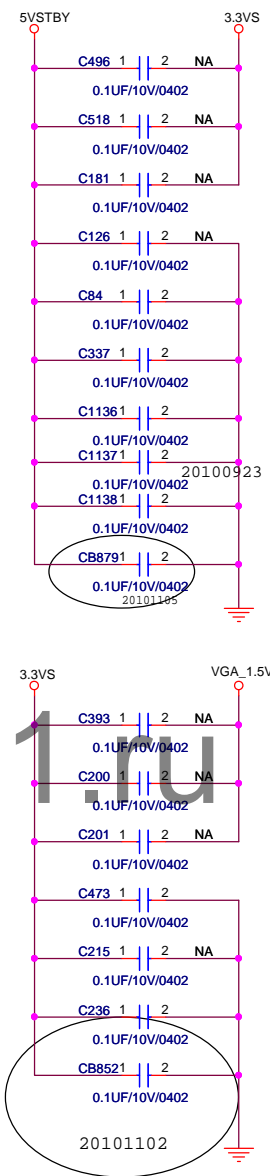
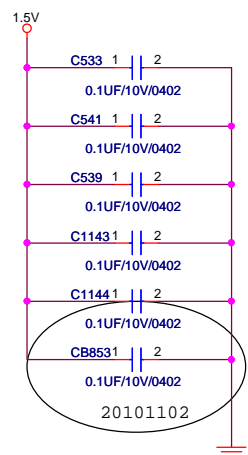
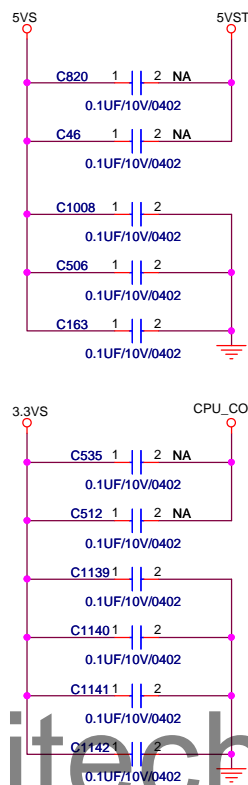
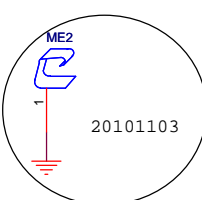
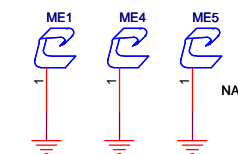
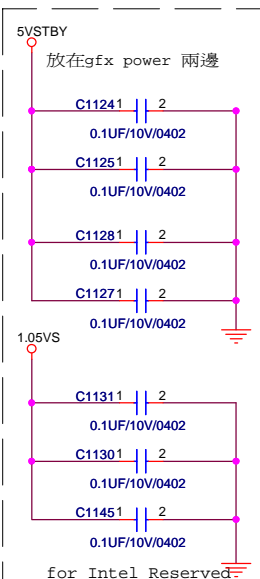
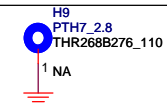
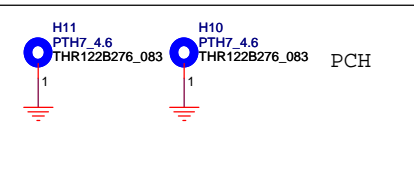
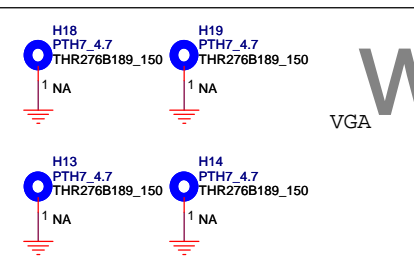
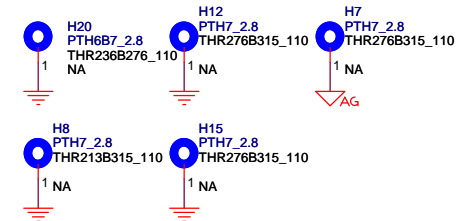
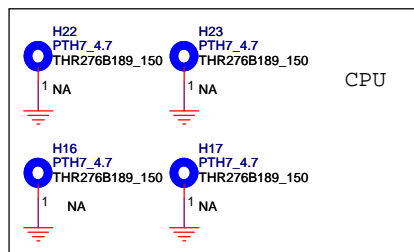
FID804 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID801 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID10 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID803 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

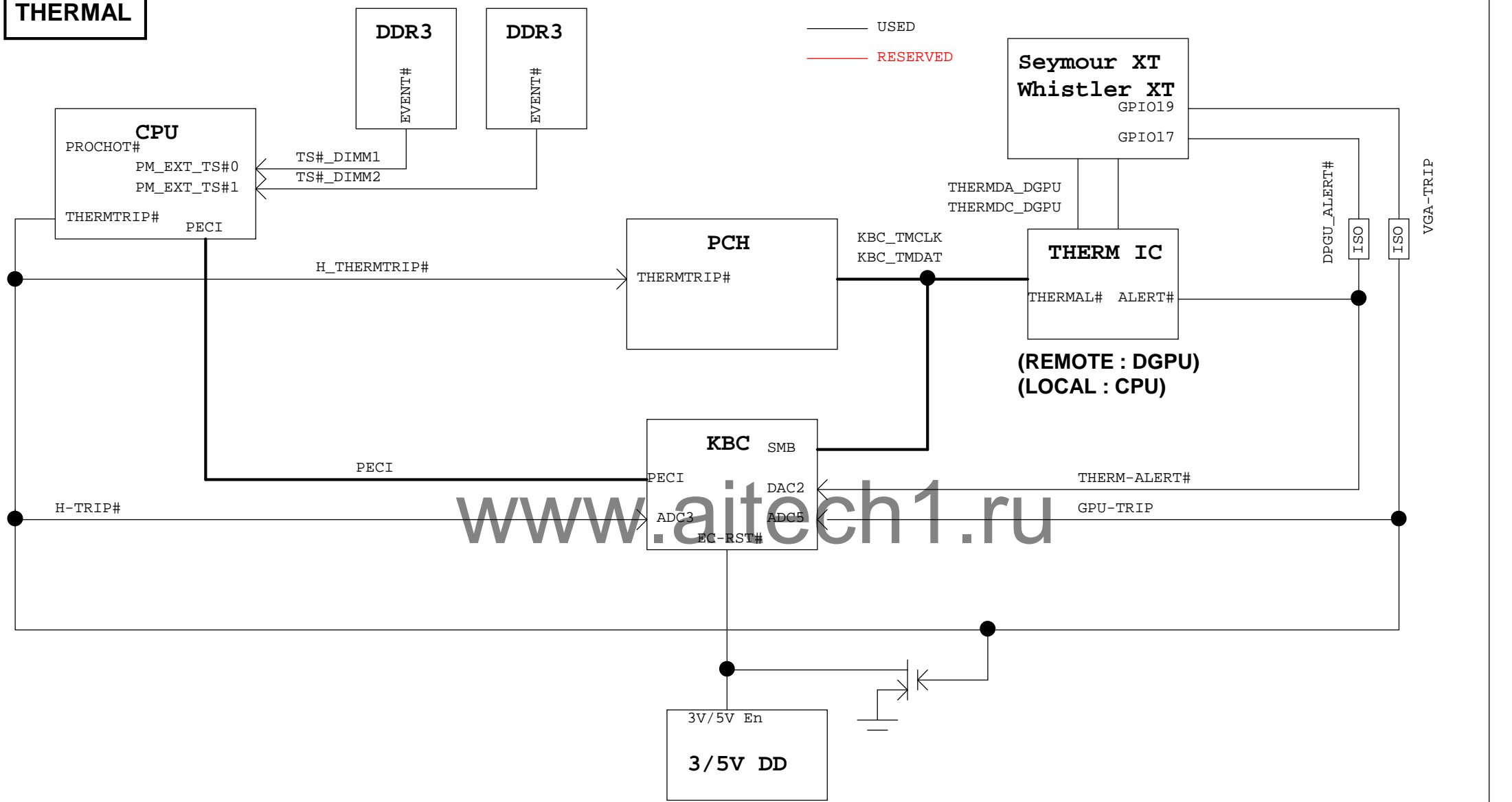
FID7 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.



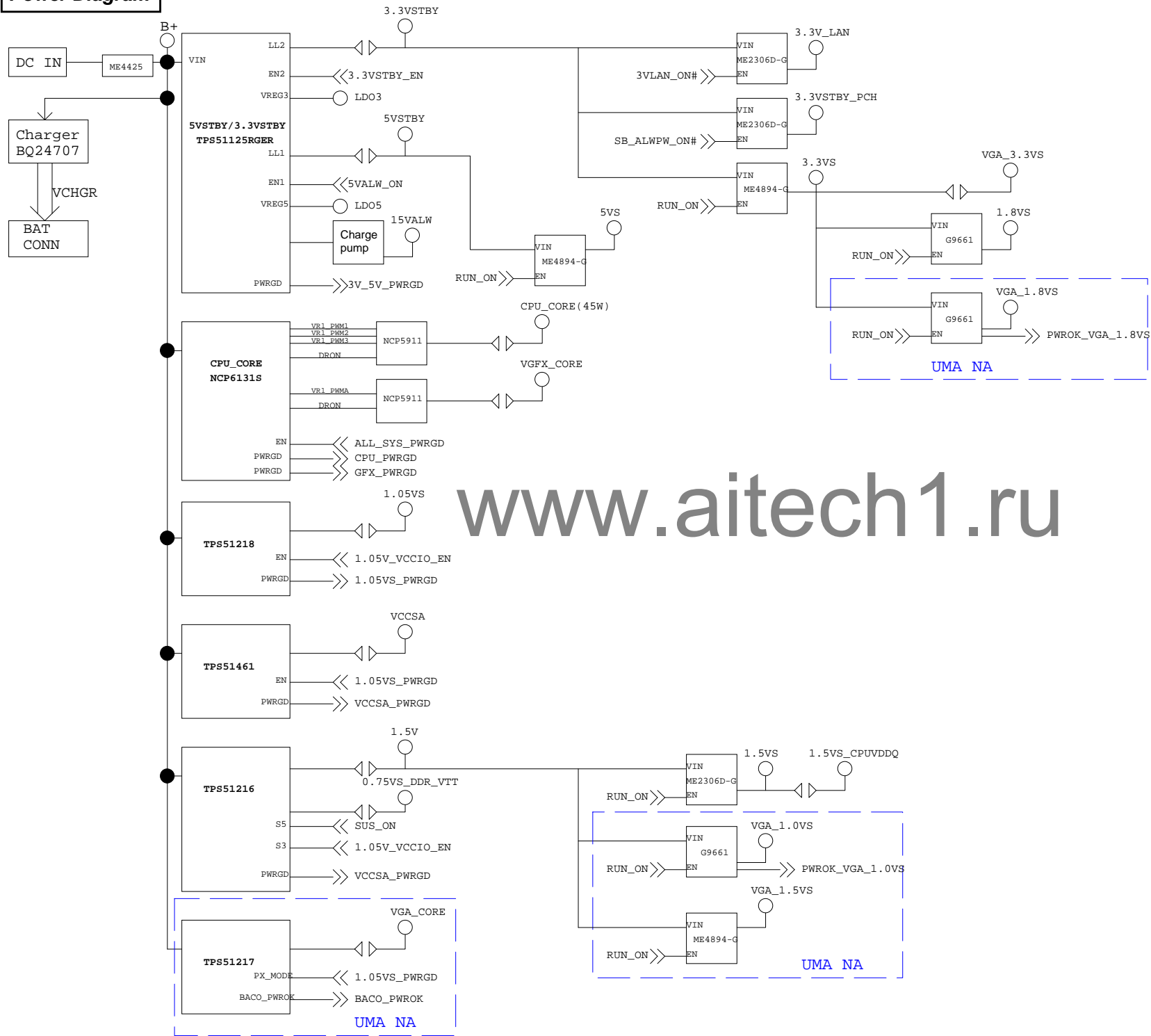
FLEXComputing

Project Name : H710D11		Title : PAD_SCREW_ Moat Cap	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet: 58 of 63	

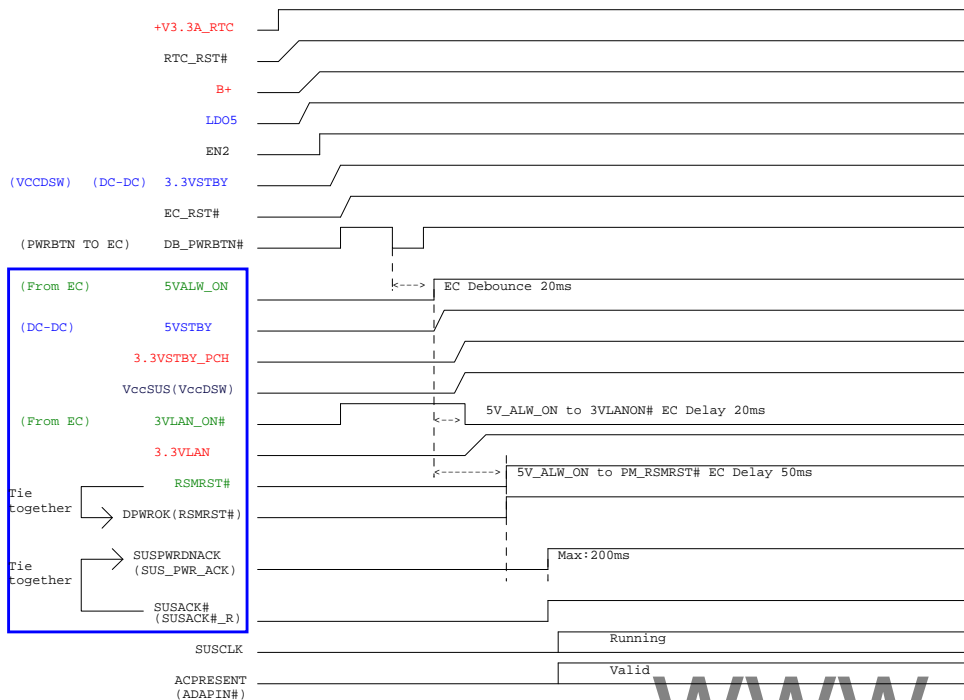
THERMAL



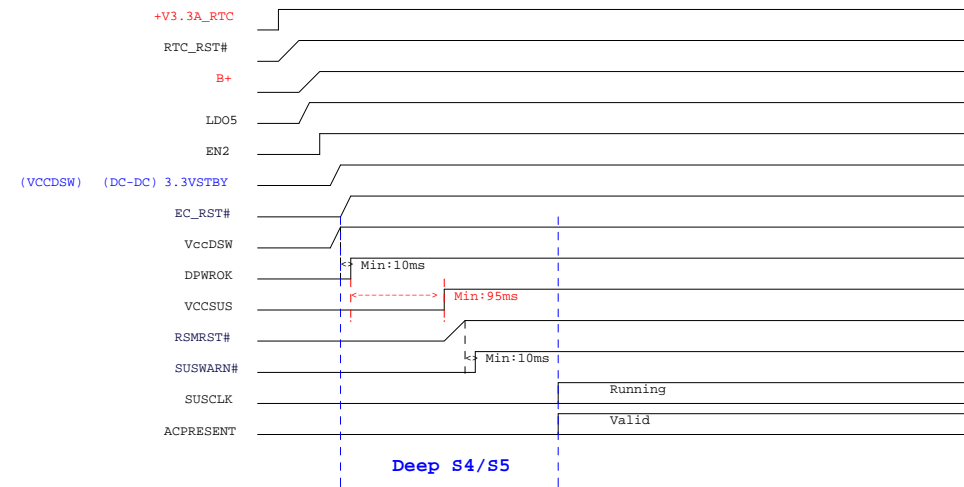
Power Diagram



G3 to S0 (without Deep S4/S5)

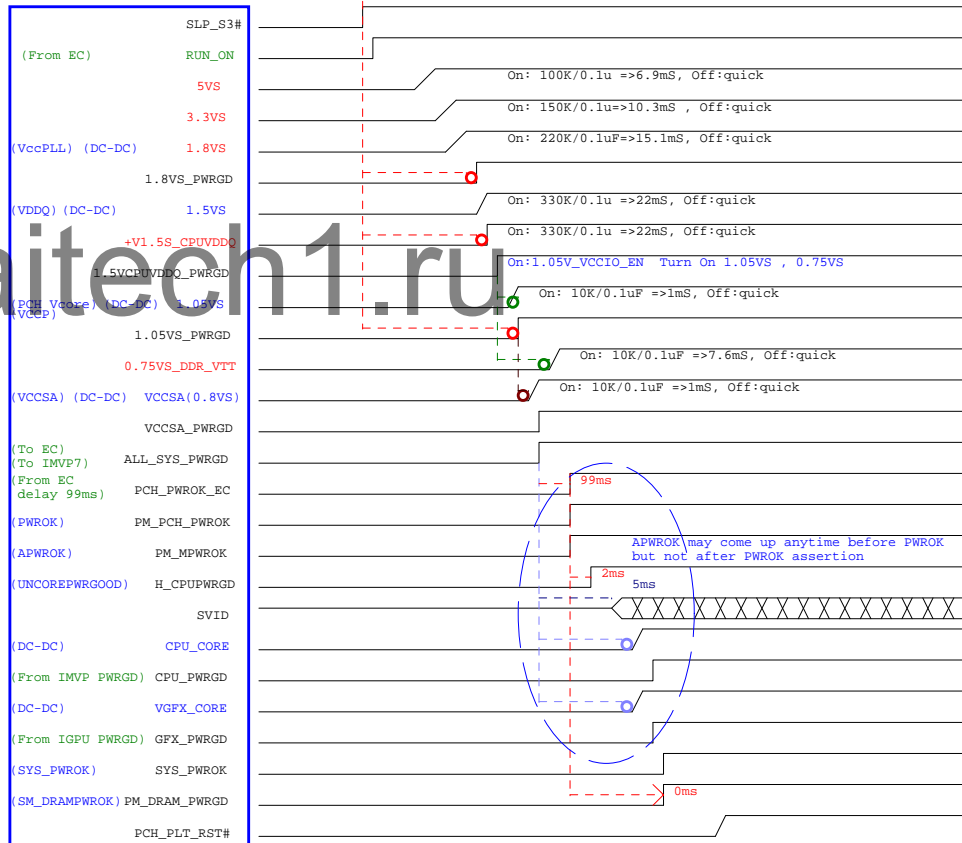
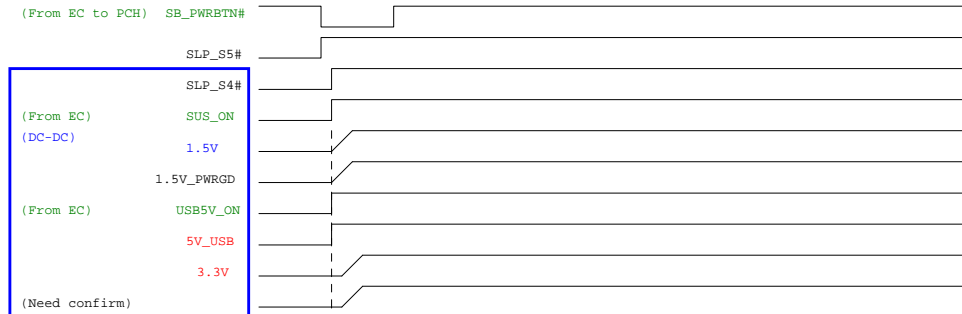


G3 to Sx (support Deep S4/S5) This Platform Without SUPPORT

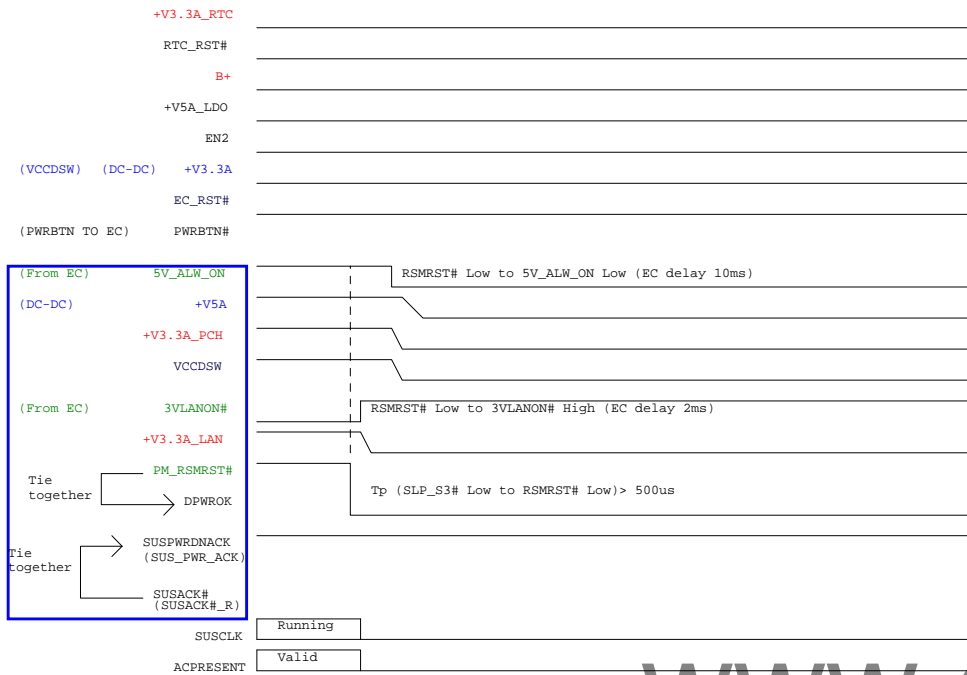


Blue: PWM
Green: EC
RED: MOSFET or Others

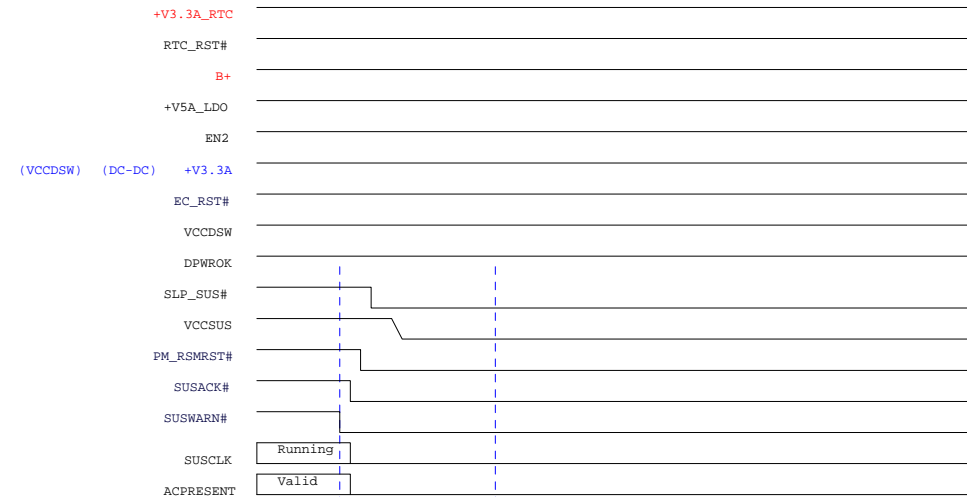
S5 to S0



S0 to S5 (WoLAN Disable) (without Deep S4/S5)

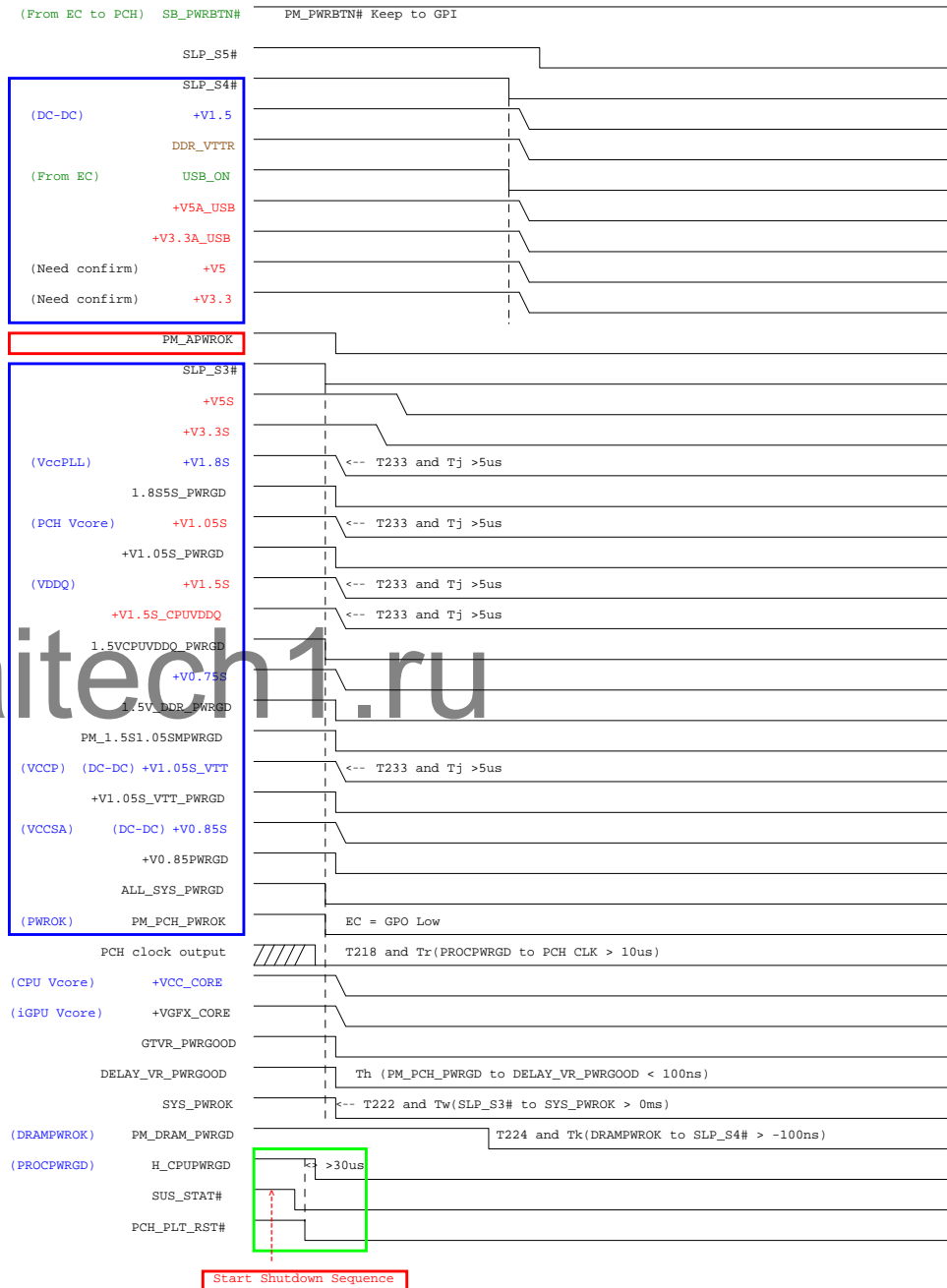


S0 to S5 (support Deep S4/S5)



Deep S4/S5

S0 to S4/S5



Start Shutdown Sequence

Blue: PWM
Green: EC
RED: MOSFET or Others

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